COTS JOURNAL®

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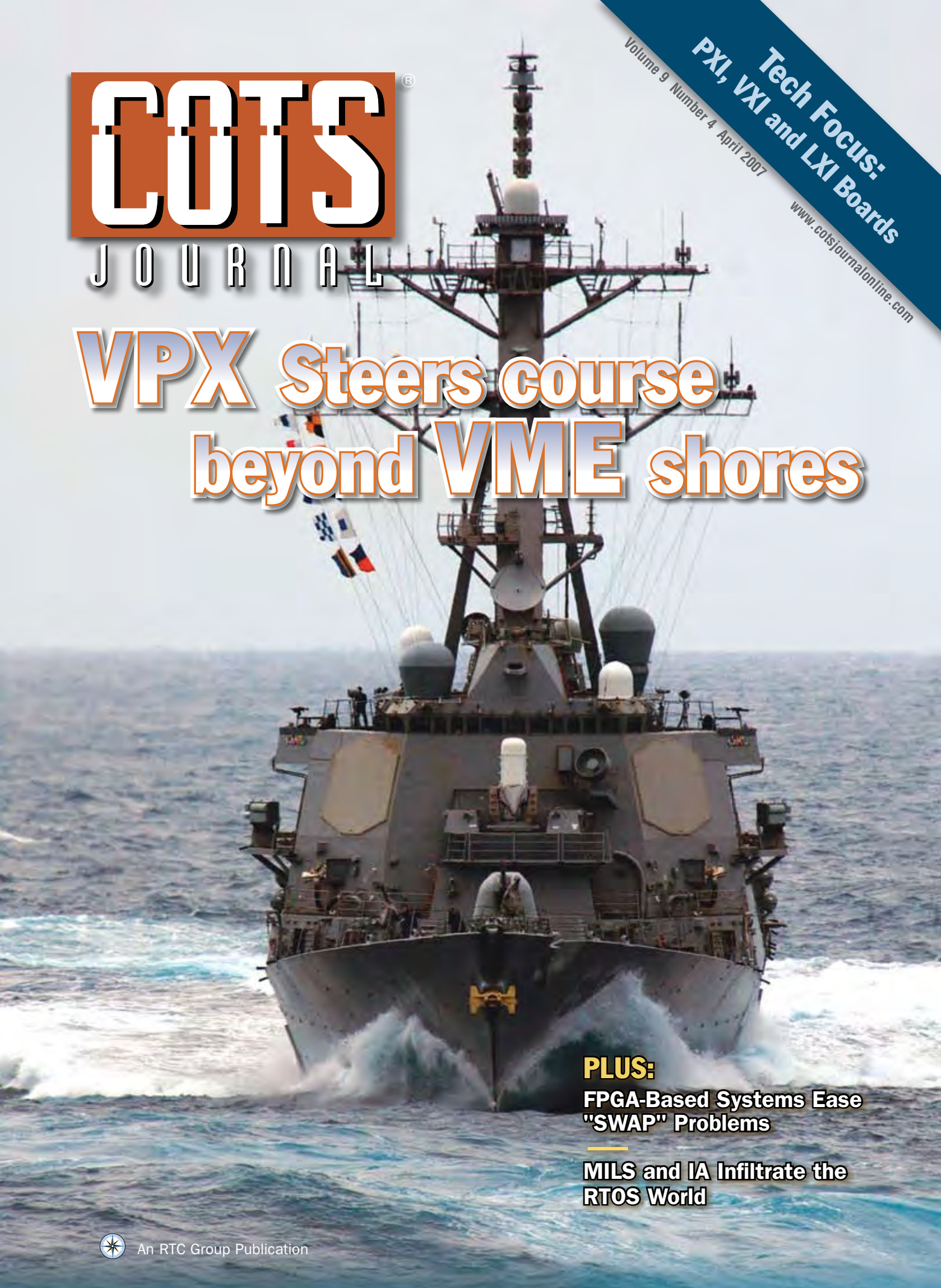
Tech Focus: PXI, VXI and LXI Boards

VPX Steers course beyond VME shores



PLUS:

FPGA-Based Systems Ease "SWAP" Problems

MILS and IA Infiltrate the RTOS World

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COM 3	RS–232	NA	RS–422/485
COM 4	RS–232	NA	RS–232
COM 5	RS–232/422/285	NA	NA
COM6	RS–422/485/TTL	NA	NA
LPTI	0	0	1
EIDE	2	2	1
USB	2	6	2
CRT	1600 X 1200	1280 X 1024	1280 X 1024
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COTS JOURNAL

Features

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Departments

Coming in May...
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Special Feature

Next-Generation VME

Tech Recon

FPGAs and Reconfigurable Computing Boards

System Development

MILS and Information Assurance

Technology Focus

PXI, VXI and LXI Boards

COTS (kots), *n.* **1.** Commercial off-the-shelf. Terminology popularized in 1994 within U.S. DoD by SECDEF Wm. Perry's "Perry Memo" that changed military industry purchasing and design guidelines, making Mil-Specs acceptable only by waiver. COTS is generally defined for technology, goods and services as: a) using commercial business practices and specifications, b) not developed under government funding, c) offered for sale to the general market, d) still must meet the program ORD. **2.** Commercial business practices include the accepted practice of customer-paid minor modification to standard COTS products to meet the customer's unique requirements.

——**Ant.** When applied to the procurement of electronics for the U.S. Military, COTS is a procurement philosophy and does not imply commercial, office environment or any other durability grade. *E.g., rad-hard components designed and offered for sale to the general market are COTS if they were developed by the company and not under government funding.*

Cover Story ..... Page 14

Radar upgrades rank among the top applications driving the need for greater compute density and I/O bandwidth. The USS Paul Hamilton (DDG 60) is an Arleigh Burke-class of guided missile destroyer. All ships of this class have the AEGIS air defense system with the SPY-1D phased array radar. The Aegis SPY-1D radar has all four faces mounted on the forward superstructure. The ship is shown here during a pass in review of ships from The Ronald Reagan Carrier Strike Group.

U.S. Navy photo by Mass Communication Specialist 3rd Class Joshua Scott

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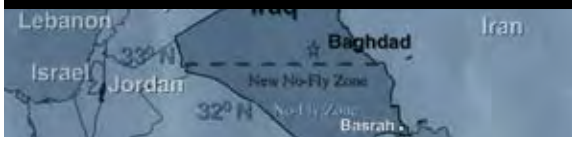
Notebook



Acquisition Reform, Déjà Vu All Over Again

In the 2007 Defense Authorization Act, Congress mandated a series of biannual reports to be produced by the Defense Department on acquisition reform. The first Defense Acquisition Transformation Report (DATR) was submitted to Congress in February. Once again Congress and the Department of Defense are saying these changes will be productive and meaningful. How many times have we heard this before? The last most meaningful change that I can remember was made in 1994 during Secretary of Defense William Perry's reign. And people and companies still are fighting his COTS initiative.

Let's give Undersecretary of Defense (Acquisition, Technology and Logistics), Kenneth Krieg a chance. He recognizes that there is a sense of urgency to get things in line, make it easier to work with the government and make whatever they do last. If you stay on top of the info that comes out of the DoD from different people, it's clear that not everyone is happy with what has been going on. And it's not fair to lay the blame entirely on suppliers. There's a lot of blame to go around: Administration, Congress, Military, Primes, and others I'm sure. Everyone has their own axe to grind in this game and that's the biggest part of the problem.

Has the Pentagon ever been able to make a long-range realistic plan of what it needs to complete its future missions and stick to it? How about a realistic timetable for delivering the new products it needs, or how much they will cost? It doesn't matter. If it rides on the ground, flies in the air or moves in the water, odds are very high that it will be late, way over budget, and not perform as originally contracted—and I don't mean over-perform. There's no need for me to reel off a long list of military programs in this column that fall under this umbrella of non-compliance. Everyone would fall asleep before you got to the end.

The heart of the DATR contains a way to incentivize contractors who deliver products that meet specified requirements, on time and within budget. The report also looks back inside the DoD to what it must do. Its personnel will have their feet held to the fire for not being realistic about program costs, schedules and deliverables meeting mandated specifications. In other words, if a proposal is too good to be true, it probably is. And you better make sure any proposal or supplier you push will come in as promised or it will affect your performance review. I wish we could do this with politicians…sorry, that thought was so tantalizing I drifted off just thinking about it.

I wonder what the plan is for programs that go for decades before deliverables start. After all, the key decision makers tend to be senior guys usually within 10 years of retirement. Maybe we can go after them in their civilian jobs and have them pay back money. But like previous plans, I applaud this latest effort to grab this Acquisition Reform Tiger by the tail and try to turn it around.

Let me step back to 1994, the last meaningful Acquisition Reform change by the DoD and something closer to home in our military embedded electronics market. In the mid-90s when the term COTS really started to catch on, marketing people from different suppliers tried to personally define COTS to meet their company's sales goals and product plans. We even had the terms ROTS (Rugged-OTS) and MOTS (Military-OTS) introduced in another effort to cut an advantage or market perception of their product versus the rest of the field. What they were attempting to do was to put an environmental or durability connotation to the word "Commercial" in the term COTS. As readers of *COTS Journal*, I know you all know that the word Commercial in COTS stands for commercial business practices and has nothing to do with the durability of the product.

I guess marketing people will always be marketing people, but recently I was leafing through a publication and came across a half dozen or more industry marketing persons who were asked to comment on the definition of COTS. Only one of the interviewees understood the definition of COTS as set by SecDef William Perry back in 1994. The scary thing is I'm not sure that any or all of the other interviewees that were trying to pin "commercial grade" to the term COTS did it for a marketing advantage. They just may not know any better.

A COTS product can be office grade or space-hardened and qualified, it can be modified to meet the specific needs of the customer, and it would not be unreasonable for the supplier to request a reasonable fee for the modifications whether the customer is an auto manufacturer or the military. So when you hear of ROTS, MOTS or any new term that tries to pin a durability grade to the term COTS, the best advice I can offer is "Reader beware." They're speaking either out of ignorance or delivering you marketing trash. ■■

Pete Yeatman, Publisher
COTS Journal

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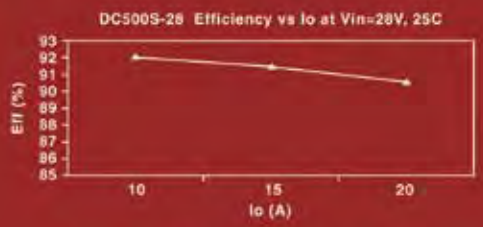

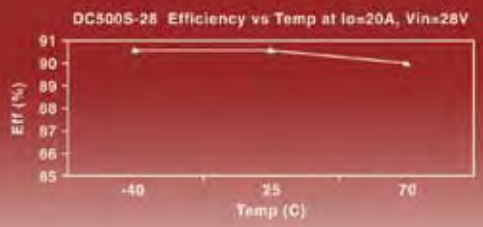

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The Inside Track

Parvus Wins Contract for Switch Router Onboard Marine EFV

General Dynamics Amphibious Systems (GDAMS) has awarded Parvus a contract for the design of the Tactical Switch Router (TSR) for the United States Marine Corps' Expeditionary Fighting Vehicle (EFV). First article prototypes of the TSR router will be delivered by Parvus later this year.

Replacing the USMC's Amphibious Assault Vehicle (AAV), the EFV serves as the primary means of tactical mobility for the Marine Rifle Squad during amphibious operations and subsequent ground combat operations ashore. Once deployed, the EFV will help the Marines sustain inland combat operations by maximizing tactical surprise; minimizing vulnerability on land; providing improved firepower, lethality and survivability; and providing on-the-move command, control, communication and computer intelligence (C4I) capabilities.

The Tactical Switch Router enables the deployment of communications-on-the-move and information-sharing capabilities, supporting the Marine Corps' net-centric operations initiatives. The TSR router is based on Parvus' DuraMAR Mobile IP router product, a rugged router system integrating Cisco System's 3200 Series Wireless and Mobile Router technology. This proven Internet Protocol (IP) networking solution enables military systems integrators to delivers secure data, voice and video communications to stationary and mobile network nodes across wired and wireless networks.

Meanwhile, in related news, U.S. Marine Corps Systems Command in Quantico, VA, has awarded General Dynamics Land Systems a $144 million contract modification for the continuation of the System Development and Demonstration (SDD) phase of the Expeditionary Fighting Vehicle (EFV) program. The contract funds the Design for Reliability (DFR) effort through September 2008.

Figure 1

The Expeditionary Fighting Vehicle (EFV) replaces the Marine Corps' Amphibious Assault Vehicle (AAV). The EFV serves as the primary means of tactical mobility for the Marine Rifle Squad during amphibious operations and subsequent ground combat operations ashore. Once deployed, the EFV will help the Marines sustain inland combat operations and provide on-the-move command, control, communication and computer intelligence (C4I) capabilities.

General Dynamics Land Systems
Sterling Heights, MI.
(586) 825-4000.
[www.gdls.com].

Parvus
Salt Lake City, UT.
(801) 483-1533.
[www.parvus.com].

Agilent Power Modules Selected for Military Radios Field Test

Defense electronics firm DME is incorporating Agilent N6700 low-profile modular power systems in its Advanced Tactical Agile Communications Test Set, or ATACTS, for testing military radios in the field. Military field technicians use the ATACTS system to determine whether a radio is usable or needs to be sent back to the depot for repair.

ATACTS combines the operations of 12 to 16 different virtual test instruments into a single, compact unit. Technicians simply plug the radio-under-test into ATACTS, and the system puts it through the predefined tests. When they were designing ATACTS, DME engineers wanted a power supply that was 1U-2U high and had three to five programmable outputs. The Agilent N6700 low-profile modular power system simplifies test-system assembly, programming, debugging and operation. Its flexibility, small size and fast command processing time make it ideal for ATE systems and production test environments.

Agilent Technologies
Palo Alto, CA.
(650) 752-5000.
[www.agilent.com].

LynxOS-178 RTOS Chosen for ESA's Galileo Satellite System

LynuxWorks has been selected to provide the RTOS for the European Space Agency's Galileo project, a civilian-controlled global navigation system. As part of the core element of the Galileo system, LynxOS-178 was the first and only commercial-off-the-shelf (COTS) RTOS to receive Reusable Software Component (RSC) acceptance for reusability from the FAA for DO-178B certification. The software will provide enhanced capabilities for communications across various devices and operating systems both on the ground and in space.

The European Galileo global navigation satellite system is designed to provide an unprecedented degree of accuracy (determining location down to the meter) and not only will have guaranteed availability, but also will be compat-

Figure 2

The ESA's Galileo Satellite Navigation System is designed to provide an unprecedented degree of accuracy—determining location down to the meter—and will be compatible with the world's other two positioning systems, GPS and Russia's GLONASS. Galileo will be used for location-based services, as well as in situations where safety is critical, such as running trains and landing airplanes, and in search and rescue operations.

ible with the world's other two positioning systems: GPS and Russia's GLONASS. Galileo will be used for location-based services, as well as in situations where safety is critical, such as running trains and landing airplanes, and in search and rescue operations.

LynxOS-178 will be used in the critical Galileo Mission Segments (GMS), which lies at the heart of the system. The GMS is a network of Earth-based stations that monitor signals from the satellites and transmit navigation data to the satellites. LynxOS-178 offers support for both Pentium and PowerPC processors, both of which will be used in the overall Galileo project.

LynuxWorks
San Jose, CA.
(408) 979-3900.
[www.lynuxworks.com].

PAM Missile Launch Paves the Way for NLOS-LS Testing

NetFires LLC, a joint venture between Raytheon's Missile Systems business and Lockheed Martin Missiles and Fire Control, successfully launched a Non-Line-of-Sight Launch System Precision Attack Missile April 4 at White Sands Missile Range, N.M., taking the missile system a significant step toward full-up missile testing planned for later this year.

After a successful launch from a tactical Non-Line-of-Sight Launch System Container Launch Unit, the Precision Attack Missile enhanced ballistic test vehicle—equipped with a telemetry system in place of a warhead and a high-fidelity mass stimulant seeker—completed the launch sequence and transitioned to flight. The enhanced ballistic test vehicle missile's wings and fins deployed, the Non-Line-of-Sight Launch System navigational system successfully operated, and the thrust vector control system and control actuator system controlled the airframe. Additionally, the telemetry system, battery system, air data system and propulsion system functioned properly.

The Non-Line-of-Sight Launch System is one of the 14 Future Combat System's (FCS)

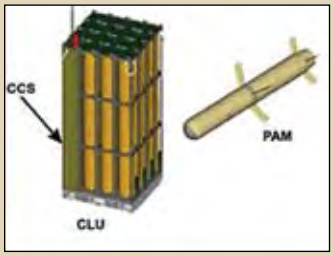


Figure 3

The Non-Line-of-Sight Launch System (NLOS-LS) is designed to give Army and Marine Corps soldiers the same capabilities that precision-guided munitions have brought to Air Force, Navy and Marine Corps aviators. It is a concept for a vertical-launch set of missiles with a command and control system in a box. Being in a box means NLOS-LS can be mounted on a Humvee or a truck, or set up on the ground.

core systems. It will operate as a part of the FCS systems-of-systems to meet the requirements of the Army's Future Brigade Combat Teams and provide increased capability for the current force's modular Brigade Combat Teams. It is also one of the key littoral combat ship mission modules.

Raytheon Company
Waltham, MA.
(781) 522-3000.
[www.raytheon.com].

Insitu Selects RTI for Unmanned Air-Vehicle Products

Insitu, a developer of long-endurance UAVs, has selected Real-Time Innovations' real-time messaging middleware for use in Insitu's next generation of UAVs, including the company's next-generation ScanEagle (Figure 4) and newer platforms.

Insitu is using RTI Data Distribution Service in multiple portions of platforms, such as on the UAV, in the ground control stations (GCSs) and in future air-to-ground communications. On the UAV airframe, RTI connects the flight computers, sensors and onboard application computers. Within the GCS, RTI connects the systems that decode data feeds, analyze the UAV's situation and interface to the operator control. Insitu's newly designed distributed software architecture allows developers to put much more intelligence on the airplane. The design leverages RTI's message bus to implement a hierarchical control network with well controlled data-flows. The information flow is now much more orchestrated and flexible than in Insitu's previous designs. For instance, this allows Insitu to seamlessly switch control between multiple GCSs and to

Figure 4

In the ScanEagle UAV, RTI's middleware connects the flight computers, sensors and onboard application computers. Insitu is using RTI Data Distribution Service in multiple portions of platforms, such as on the UAV, in the ground control stations (GCSs) and in future air-to-ground communications.

reliably connect to an aircraft even over unreliable links.

RTI Data Distribution Service (formerly NDDS) is high-performance messaging middleware for the development and integration of distributed real-time applications. It provides low latency, high throughput, high scalability, deterministic response and full control over network, processor and memory utilization. RTI Data Distribution Service complies with the Object Management Group (OMG) Data Distribution Service for Real-Time Systems (DDS) standard.

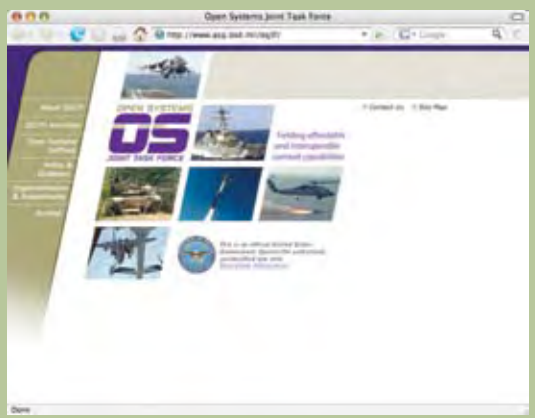
Real-Time Innovations
Santa Clara, CA.
(408) 200-4700.
[www.rti.com].

COTS Websites

www. acq.osd.mil/osjtf

Open Systems Concepts Converge at OSJTF Web Site

The concept of open systems ranks as one of the core enablers of the COTS movement. Open system architectures not only make it easier to mix and match subsystems from several different commercial vendors, they also streamline the process of technology refresh. In fact, open systems are so vital to today's military system development, that the Department of Defense created the Open Systems Joint Task Force (OSJTF), chartered as a cooperative effort of the Department of the Army, the Department of the Navy, the Department of the Air Force and the Office of the Under Secretary of Defense (Acquisition and Technology). The group is tasked to sponsor and accelerate the adoption of an open systems approach for new systems and system upgrades.



To support that goal, the OSJTF's Web site offers a wealth of resources to help developers of military systems educate themselves on open systems standards and concepts. The site also serves as a portal to network with the various DoD and industry entities involved in open systems. Visitors to the site can access various standards and policy documents related to open systems. A complete indexed library on the site offers downloaded open systems resources files in Power Point, MS Word and PDF formats. A Points of Contact page provides contact info for each military branch that's part of OSJTF. The site provides links to numerous educational resources including course information, conferences and links to several open-systems-based trade associations and standards bodies.

Open Systems Joint Task Force
Arlington, VA. (703) 602-0851.
[www.acq.osd.mil/osjtf].

Special Feature

Next-Generation VME

Hurdles Behind it, VPX Hits Its Stride

With VPX now gaining momentum, the debate over next-generation VME has shifted. With VPX/VPX REDI closer to reality, the role of VXS as a "here now" alternative is in question.

Jeff Child
Editor-in-Chief

There's a healthy irony in the fact that this, the year following VME's 25th anniversary, is settling in to be the "Year of VPX." It's ironic because VPX is armed to eventually displace traditional VME and break its long legacy of complete backplane backward compatibility. This won't happen overnight by any means. In fact, VME board vendors report that old VME64 remains the dominant flavor of VME shipped today, and that won't change for some time. But VPX is shaping up to have what it takes to make even the most entrenched military system designer consider doing the unthinkable and upgrade to the VPX switched fabric-based backplane.

A broad characterization can be made about what military applications are driving the early interest in VPX. There's a strong trend toward radar systems of all kinds—ground-based radars, air and naval radars, airborne recon radars (Figure 1)—that are hungry to run compute-intensive, data-intensive applications, and they want to use Serial RIO on the backplane. VPX lets them do that with enough high-speed connectivity so they don't need a centralized switch, but instead use a distributed switching approach.

The other big area that seems to be flocking to VPX is Electronic Warfare. Sometimes moving even more data than a radar does, EW systems need to sweep a wide band and they need to distribute

Figure 1

Developers of new advanced, integrated radar systems are among the front ranks of VPX early adopters. Shown here, U.S. Army Lt. Col. Jim Roman (right) and Army Sgt. 1st Class Steven Jamie, both aboard a E-8C Joint Surveillance and Target Attack Radar System aircraft, talk about the timing of communications to Army ground units in Iraq *(U.S. Air Force photo by Master Sgt. Lance Cheung).*

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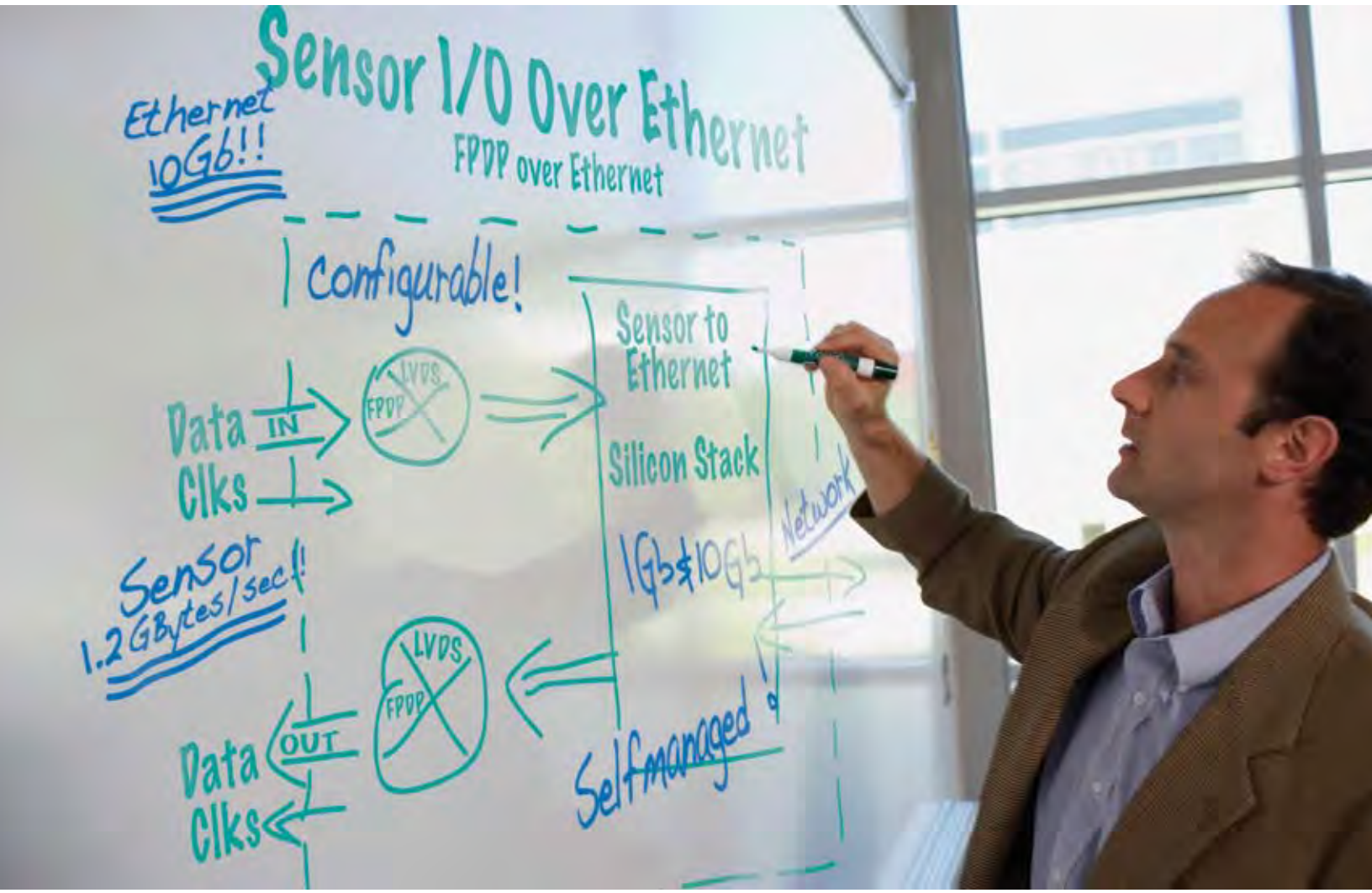

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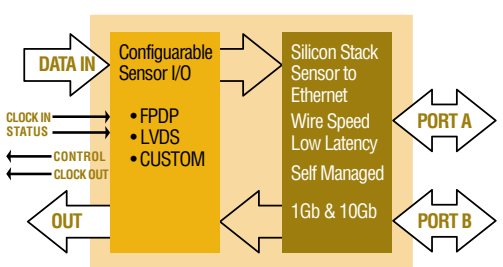

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masses of data to multiple processing cards, and store it as well. Meanwhile, the goal is always to squeeze the same capabilities in a smaller space—take two boxes and make it one— three and make it two—and then immediately use that freed-up space for another sensor array or extra comms gear perhaps. VPX blends the high speed, integration and I/O density to make all that possible.

Just a few years ago, and well into last year, the landscape of next-generation VME was quite different. The debate was split fairly evenly in the industry between those that believed VITA 41 (VXS) was the best "here and now" performance follow-on to VME, and those that preferred to skip over an interim solution like VXS and move directly forward with VITA 46 (VPX). With ANSI approval in place for the base VXS spec ANSI/VITA 41.0, ANSI/VITA 41.1 InfiniBand, and for ANSI/VITA 41.2 RapidIO, VXS certainly had a good jump on VPX. And several vendors have first and second rounds of VXS products already on the market and doing well (Figure 2).

Base VPX Spec Finalized

What's changed in recent months is that VPX has shaken loose from the perception as "next-decade" technology, and looks on its way to claim the same "here and now" status boasted by the VXS camp. A major milestone was achieved by the VITA 46 (VPX) Working Group in February when it came to an agreement on the 46.0 Base spec. The group declared 46.0 finished from the Working Groups' perspective and began the process for ANSI ratification ballot of the spec. That expands the number of people within the VITA community that can evaluate it and then vote to approve it. Stewart Dewar, Chair of the VITA 46 Working Group said, "We are within some small number of months of achieving ANSI standard status for the basic 46.0 spec. That's a major achievement that we've been working on for years now."

Beyond the Base 46.0 spec for VPX, there's a number of subsidiary VITA 46 specifications that are part of the hierarchal VITA 46 spec family. The two switched fabric pinout specs—for Serial Rapid IO and PCI Express—are the most important ones. It's expected to be mid-year before those are finalized. Other less "core" subsidiary specs are one that defines system management for VPX, and a standardized fiber optic interface for VPX. Those don't hold back the basic

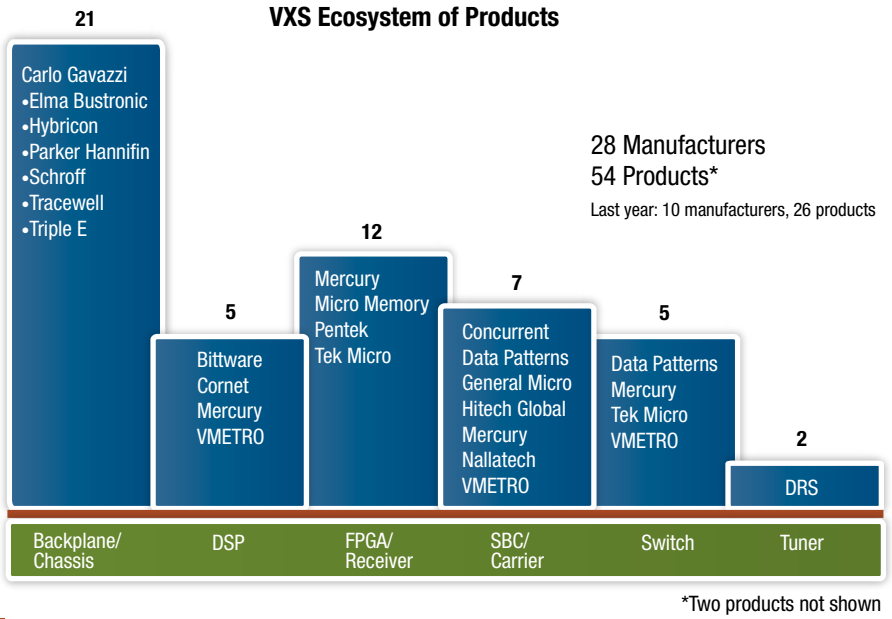

Figure 2

Among VXS's advantages is its established ecosystem of products. At last count, taken earlier this year, VXS has 54 products from 28 vendors.

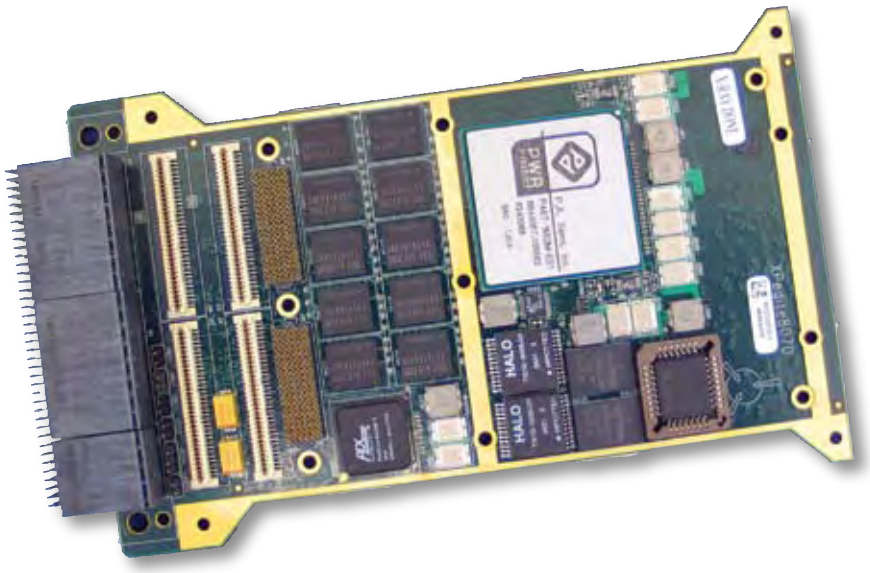

Figure 3

An example VPX board is Extreme Engineering's XPedite8070, a high-performance 3U VPX-REDI single board computer. With two PA Semi PA6T cores running at up to 2.0 GHz while dissipating less than 17W, the PA6T-1682 delivers optimum performance per watt. The board sports optional support for PCI Express, 10 Gigabit Ethernet XAUI and Gigabit Ethernet P1 links.

product roll outs that have been underway, but they are enhancements that were part of the pre-planned vision for VPX.

The system management spec adds a twist not seen in the embedded military market before. ATCA, for example, has the system management as part of the spec, because there's more of a tradition of system management within that data center, enterprise computing environment. In contrast, there really is zero tradition of system management in embedded military/aerospace realm, which is one reason that particular VPX subsidiary spec is taking longer, says one member of that Working Group.

VPX, but Which Fabric?

One of the hurdles slowing the acceptance of VPX has been fears of a mini-fragmentation with VPX. That's because VPX supports a variety of interconnect technologies. The choice is a two-edged sword. In one way those options expand the applicability of VPX to different applications. On the other hand, because of those options, many are somewhat cautious about adopting what appears too flexible to be called a true standard. Fortunately what's emerging is a de facto standard around a mix of Serial RapidIO and PCI Express. Curtiss-Wright and GE Fanuc have gone that route in the VPX boards so far introduced to the market. There's also a degree of switched fabric compatibility inherent in VPX. With four fabric ports on a VPX board, each one can be independent. For example, port number 4 could be switched from Serial RapidIO to PCI Express (or vice versa) without interfering with the way the other three ports work. It doesn't take a board redesign to switch from one to another.

VPX does require users to throw out their old VME backplanes and replace it with a VPX one. That may be a hard reality to bear, but the good news is that there's a way to still make use of legacy VME boards in a VPX system. The VITA 46.1 provides a definition for mapping VME to a VPX backplane. It provides a standardized pinout that defines where to put VME on a VPX backplane. Early adopters—quite a number of them—are reportedly planning to implement mixed systems that leverage the 46.1 mapping.

VPX Products Roll

Further fueling VPX's momentum, recent months have seen a slew of product and roadmap announcements from board vendors. At an industry event in January, seven leading chassis and embedded board vendors rolled out their VPX roadmaps or showed existing VPX products. Among the seven were Curtiss-Wright, Elma Electronic, GE Fanuc (formerly Radstone), Hybricon, Mercury, Micro Memory and Parker Hannifin. Since then, VMETRO and Extreme Engineering (Figure 3) have likewise rolled out a VPX roadmap and VPX product respectively. For its part, Curtiss-Wright presented at the event the first public demonstration of an embedded system based on VPX.

The demo comprised a system using several new 6U form-factor VPX boards. The system featured a VPX6-185 single board computer (SBC) and two CHAMP-AV6 DSP VPX boards operating in a mesh Serial RapidIO (SRIO) network. Each board in the mesh was connected to each of the others by a bi-directional x4 SRIO connection, with each link providing up to 2.5 Gbytes/s of bi-directional bandwidth. The demo system is shown in Figure 4. An application running on the system enabled viewers of the demonstration to choose the number of processors participating in simultaneous streaming transfers between the boards. This application is representative of common signal processing algorithms associated with radar processing, which are often limited by data movement in traditional systems. ■■

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Figure 4

Earlier this year Curtiss-Wright presented the first public demonstration of an embedded system based on VPX. The demo featured a VPX6-185 SBC and two CHAMP-AV6 DSP VPX boards operating in a mesh Serial RapidIO network. Each board in the mesh was connected to each of the others by a bi-directional x4 SRIO connection, with each link providing up to 2.5 Gbytes/s of bi-directional bandwidth.

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Special Feature

Next-Generation VME

Choices for Mil/Aero System Designs: VXS vs. VPX

VXS and VPX are vying for acceptance as the follow-on to traditional VME military applications. Understanding where they're similar and where they're different is key to choosing which direction to go in.

Justin Moll, Director of Marketing
Elma Bustronic

The most basic and standard backplane configurations of VXS (VITA 41) and VPX (VITA 46) can seem a world apart. But in some designs it begins to be difficult to see the differences in performance and function of the two specifications. Actually, "standard configuration" is somewhat of an oxymoron for VPX. One of the key features of the specification is its flexibility. The architecture can simultaneously support a mix of bus segments including full mesh, pipeline or single or dual star topologies. Mesh is the typical topology for VPX.

The system designer can use exactly as many pins and connection configurations, etc., as are needed for the specific application. The VITA 46 specification provides a standard card layout and standard mechanics. From there, the system engineers can pick and choose the connections between them to meet the exact needs of the application.

VXS, on the other hand, is a more defined approach. The specification starts with a specific pinout, with some undefined pins for I/O, and so on. Customization can be implemented in the undefined areas or in different configurations without violating the specification. With VXS, the layouts are fairly defined for star—one hub slot—or dual star (two hub slots) topologies. Vendors can create interoperable standard hub and payload cards based on the specification that will work in all kinds of VXS backplane configurations.

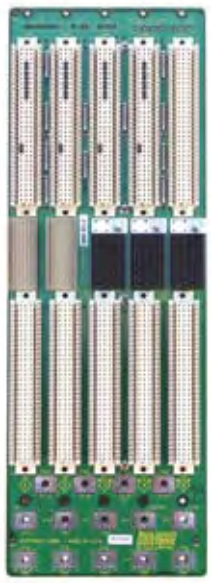

Figure 1

This VXS backplane has two legacy VME64x slots on the left side. Typically, there would be a switch card slot. However, this backplane has a point-to-point mesh connection across the P0 pins.

Backward Compatibility

Further, the VMEbus backward compatibility is always an option. Many existing VME or VME64x cards can be re-used or upgraded with little effort. Although the P0 connector is different in VXS from the VME64x P0 connector, not all VME cards use the P0, and a hybrid backplane can always be implemented (Figure 1).

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VPX can also achieve compatibility with legacy VME in hybrids. The VMEbus can be routed across the high-speed MultiGig connectors to legacy VME64x slots. Figure 2 shows an example along those lines. Both VXS and VPX are well suited to Mil/Aero applications. They both are based on the rugged Euro-card form-factor. The proponents of the architectures come from the VME community—experts in serving the needs of rugged applications.

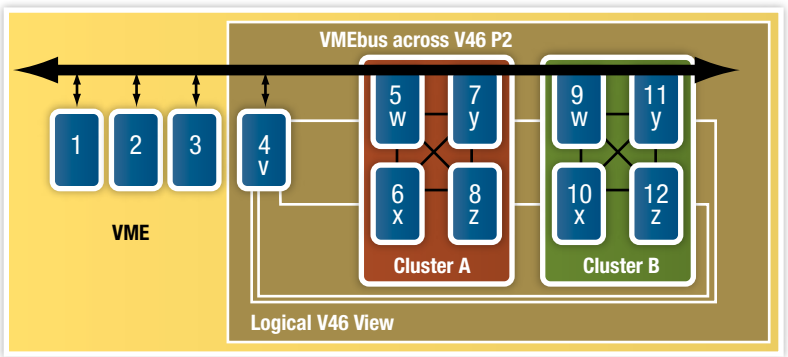

Figure 2

The diagram shows how the VME can be incorporated into the VPX backplane and connected across all slots.

Key Differences

Let's look at some of the key differences between VXS and VPX. First, VPX can be designed in a 3U backplane format. This combination of performance in a small form-factor may be a very attractive feature for many Mil/Aero applications. VXS and VPX use the same high-speed MultiGig connector family for the differential pair routing. But, the backplane pitch (distance between the slots) for VXS is typically 0.8" and VPX is 1.0". So, VXS allows 21 slots in a 19" rack. (Note: the max slots for a dual star VXS due to number of pins is 20 slots, however, the designer can use 1 legacy VME64x slot for a total of 21 slots.) VPX allows a maximum of 16 slots at

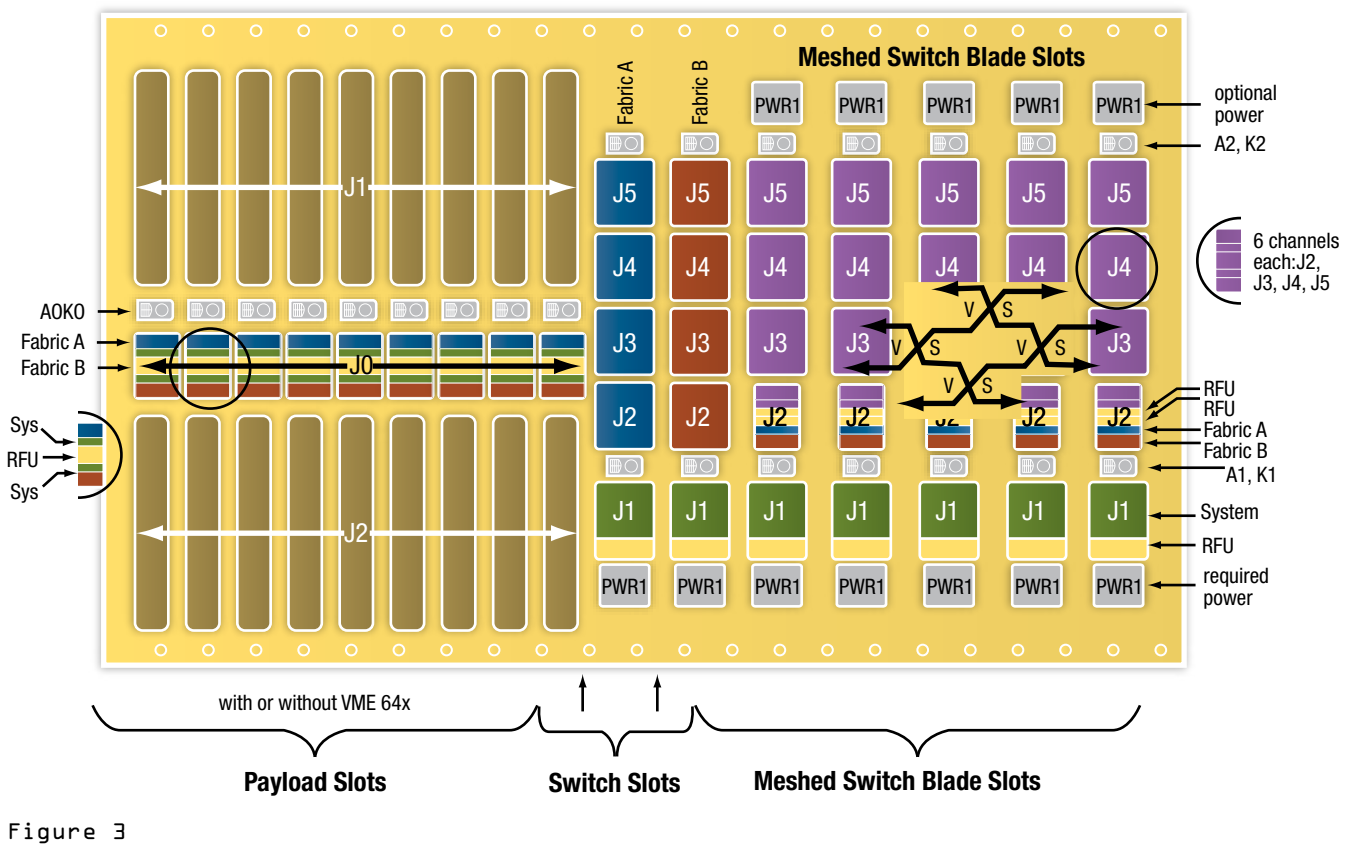

Figure 3

The layout of a Processor Mesh backplane with mesh slots, centralized switch slot, payload slots and central I/O slot.

1.0" pitch in a 19" rack—unless some of the slots are legacy VME64x slots at 0.8" pitch. Other differences include the power input options, number of I/O pins, alignment/keying pins, and more. A typical mesh VPX offers more bandwidth—5,000 Mbytes/s slot-to-slot—versus a typical dual star VXS—3050 Mbytes/s slot-to-slot.

For I/O, VXS has 110 undefined pins available in the J1/J2 connectors and 135 P0 pins. However, VPX has 480 pins per slot that could be assigned by the user or they could be used as up to 192 differential pairs. This is because the connectors J1 - J6 have no required (defined) use.

VXS has a larger ecosystem with 44 products from 16 different manufacturers at the time of this writing. VPX is a younger specification, so its ecosystem is still growing. There are three card vendors with announced products and another on the way. There are at least two backplane/chassis vendors, with another concept/demo unit by a third party.

Is that VXS or VPX?

Where the lines really start to blur between VXS and VPX is with VXS Processor Mesh and VPX hybrids. VXS Processor Mesh is an innovation created by Elma Bustronic. Much like VPX, it offers a mesh configuration over VXS. Why not? They use the same high-speed connector family.

VXS Processor Mesh is a powerful architecture with bandwidth that can deliver 112 Gbits/s of aggregate throughput within the processing mesh in a single chassis. This is a 6x improvement over standard star or dual star VXS topologies. Each switch slot in Processor Mesh implements twenty x4 links for a total of 25 Gbits/s per switch slot. The addition of a fat-pipe processor fabric segment further enhances the other key features of the VITA 41 architecture such as I^2C management bus, backward compatibility to VME64x, PMC/XMC mezzanine sockets, rear transition slots, and the rugged VME64x mechanical architecture. As Processor Mesh VXS is a point-to-point mesh without the complexity of a switched fabric, it is natural to use

VITA 41 VXS Versus VITA 46 VPX: A Comparison

	VITA 41	VITA 46
Form Factors	6U	3U, 6U
Performance Maximum (Theoretical)	Star/Dual Star: 30 Gbps Processor Mesh: 112 Gbps	112 Gbps
Topologies (Typical)	Star, Dual Star (Payload Mesh and Processor Mesh also possible)	Mesh
Cooling Mechanicals	Convection (IEEE1101.10/11), Conduction (IEEE1101.2)	46.1: Convection (IEEE1101.10/11), 46.2: Conduction (IEEE1101.2), 46.3: Liquid Flow Through
Electrical Architecture	VME64x Serial Fabric System Management	VME64x Serial Fabric System Management
Signaling Protocols	VME, IPMI, I2C Ethernet, Serial Rapid IO PCI Express	VME, IPMI, I2C Ethernet, Serial Rapid IO PCI Express
Backward Compatibility	VME, VME 64, VME64x, IEEE 1101.2, VITA 48 PMC, XMC, VITA 56 (only on payload cards)	Not direct, but hybrid interface defined IEEE 1101.2, VITA 48, PMC, XMC, VITA 56
Minimum Payload Defined	2 channels	N/A
Fixed slot signal assignments	Yes	No
Slot pitch	0.8" payload slots / 0.8" or 1.0" for switch slots.	1.0" typical
User IO	Switch - 18 Payload channels, 4 inter-switch channels, 2 reserved channels. + 121 additional single ended signals (15 permanently assigned to system utilities) Payload – 2 fabric channels + 30 single ended signals and 5 single ended signals permanently assigned to system utilities	Flexible assignment of connectors for either single ended or differential use. Assignment to fabric or I/O depends is never fully defined. See maximum channels.
Connector System Backplane Connector System Daughter Card	Switch: 9-column – MultiGig backplane connector 12-column – MultiGig daughter card connector Payload: 9-column – MultiGig backplane connector 7-column – MultiGig daughter card connector	9-column – MultiGig backplane connector 7-column – MultiGig daughter card connector
Maximum channels *	Switch - 192 total differential pairs / 24 bi-directional 10Gbps channels (assuming 2.5 Gbps per pair) Payload – 16 differential pairs / 2 bi-directional 10Gbps channels (assuming 2.5 Gbps per pair)	6U - 192 total differential pairs or 24 bi-directional 10Gbps channels (assuming 2.5 Gbps per pair) 3U – 64 total differential pairs or 8 bi-directional 10Gbps channels (assuming 2.5 Gbps)
Voltages required	5 VDC - VXS 5, 3.3, +12, -12 VDC - VME for VME enabled payloads	All Optional: 5, 12 or 48 VDC
Current announced product as of writing	32 boards	3 boards

** The number of I/O channels given is based upon the total number of differential pairs defined in the two base standards (VITA 41.0 and 46.0). The subsidiary documents assign these differential pairs to various uses so users should consult the specific subsidiary implementation to determine how the differential pairs may be used.*

Table 1

Show here is a comparison chart of VXS, VXS Processor Mesh and VPX.

SERDES-based signaling protocols. Because bandwidth-intense processes can now be offloaded to the VXS Processor Mesh, the conventional two-channel central switch fabric defined by VITA 41.0 may be used primarily for a control and I/O pathway.

This means less expensive switch cards may be used to support the star or dual star switched fabric and the more powerfully equipped processor-switch engines may be reserved for signal processing and computational tasks. VPX Processor Mesh, legacy VME64x slots, standard VXS slots and processor mesh slots can all be used in the same backplane. Therefore, backward compatibility is still an important element of the solution. The architecture is in draft as VITA 41.7 with defined pinouts. The theoretical performance of Processor Mesh is 7500 Mbits/s slot-to-slot.

So, what are the differences in performance and features in VPX and VXS Processor Mesh? VPX offers a larger mesh configuration than Processor Mesh, but performance slot-to-slot is comparable between the two. Processor Mesh offers the benefits of VXS—compatibility, defined pinout, large ecosystem. Table 1 shows a comparison between VXS and VPX.

VPX-REDI

When VPX-REDI is available, it will offer very impressive performance. With 48V cards at up to 16 amps, the slots could potentially require up to 768 W/slot of cooling. Conduction- or convection-cooling schemes will not be able to handle some of these high power and density applications for VPX. To handle this extreme environment, the cards will utilize liquid flow-through cooling in metal encased modules. The differences between VXS and VPX will be more dramatic when the VPX-REDI cards and chassis become available in the future.

In certain VXS and VPX hybrid designs, you may see more similarities in the architecture than differences. Backward compatibility will keep VXS a mainstay in the market. Concepts like Processor Mesh help guarantee its performance evolution into the future. VPX should also be successful for many applications that need the power, I/O and bandwidth options. In the future, 3U versions may also become a key solution for applications where performance is a must and space is limited, like UAVs, Humvees, or several other Mil/Aero applications. ■■

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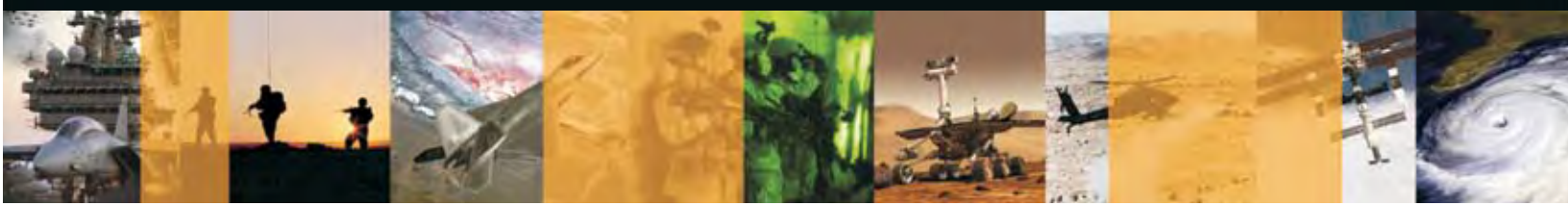

Special Feature

Next-Generation VME

VXS and VPX REDI Pave Road to Next-Generation VME

Choosing among next-gen VME choices like VXS and VPX REDI—and their subsets—calls for careful consideration of the thermal, I/O and power dissipation issues of each.

Bob Sullivan, Vice President of Technology
Hybricon

There's no question that the VME market is still strong, with a robust ecosystem, and remains the leading form-factor in shipment revenue. For the system developer who is looking to evolve from VME into higher performance form-factors, the VITA community has crafted several standards to choose from. With so many form-factor choices out there—both VITA and non-VITA—these days, systems designers must carefully consider the thermal, I/O and power dissipation issues of each alternative.

Among the most established of the next-gen VME alternatives is ANSI/VITA 31.1. The ANSI/VITA 31.1 standard, which implements Gbit Ethernet on VME64x Backplanes—was completed several years ago, but only recently achieved critical mass in the VME ecosystem with compliant boards available from several vendors.

Patterned after PICMG 2.16, ANSI/VITA 31.1 provides an Ethernet switch fabric for VME64x cards using the standard VME64x P0/J0 connector. In fact, ANSI/VITA 31.1 uses the PICMG 2.16 Fabric Slot connectors and pinout, allowing PICMG 2.16 Fabric Boards to be used for the Ethernet switching in ANSI/VITA 31.1 systems. ANSI/VITA 31.1 is a low-cost alternative that has been flying under the radar. It is a good alternative for applications that don't require the performance provided by VXS or VPX, and provides complete backward compatibility with VME.

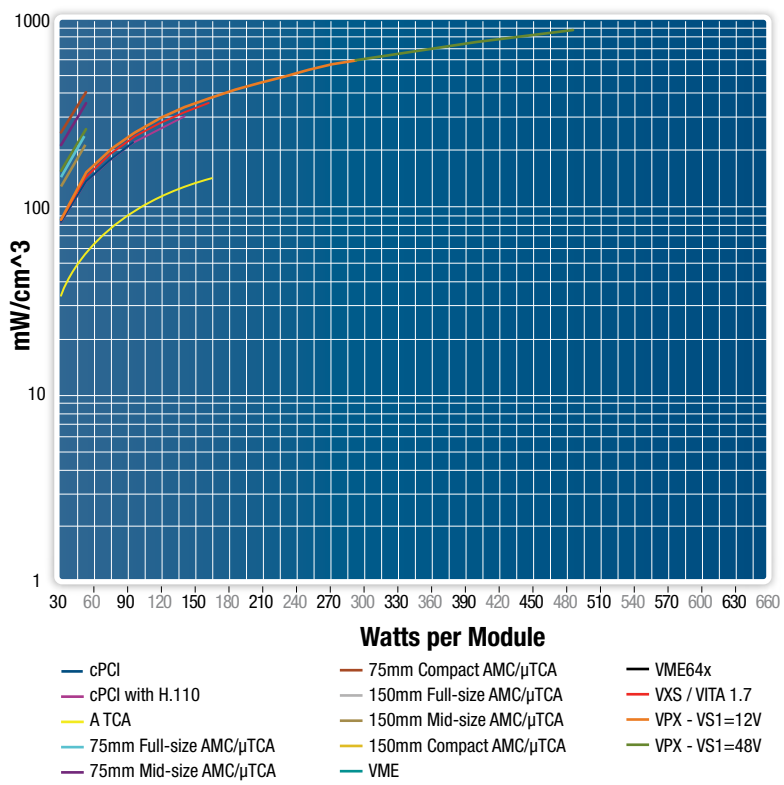

Figure 1

Shown here is the thermal density in mW/cm³ for various embedded board technologies and power levels.

VXS Market Maturing

VXS products have been in the market for several years, and the market is maturing. The VXS ecosystem is strong, with 54 board-level products from 28 vendors. This includes both air-cooled

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VXS (VITA 41) Standards and Draft Standards
ANSI/VITA 41.0 VXS Base
ANSI/VITA 41.1 InfiniBand
ANSI/VITA 41.2 RapidIO
VITA 41.3 VXS 1,000 Mbit/s Baseband IEEE 802.3 (draft)
VITA 41.4 VXS PCI Express (draft)
VITA 41.5 VXS Aurora (draft)
VITA 41.6 VXS 1X Gigabit Ethernet Control Channel Layer (draft)
VITA 41.7 VXS Processor Mesh (draft)
VITA 41.10 Live Insertion (trial use)
VITA 41.11 Rear Transition Module (draft)

Table 1

VXS is an evolution of VME, providing good backward compatibility with VME systems. Shown here are the various VXS standards and subset standards.

VPX (VITA 46) Draft Standards
VITA 46.0 VPX Base (draft)
VITA 46.1 VME (draft)
VITA 46.9 XMC/PMC mapping (draft)
VITA 46.10 Rear Transition Module (draft)
VITA 46.3 Serial RapidIO mapping (draft)
VITA 46.4 PCI Express mapping (draft)
VITA 46.20 Switch Slot Definition (draft)
VITA 46.6, 46.7 Ethernet core fabric (draft)
REDI (VITA 48) Draft Standards
VITA 48.0 REDI Base Standard (draft)
VITA 48.1 REDI Air Cooling (draft)
VITA 48.2 REDI Conduction Cooling (draft)
VITA 48.3 & 48.4 REDI Liquid Flow-Through Cooling (draft)
VITA 48.5 REDI Air Flow-Through Cooling (draft)

Table 2

VPX, with its companion REDI standards, is designed from the ground up to support two-level maintenance. Listed here is a summary of the VPX and REDI VITA standards, all of which are still in draft phase.

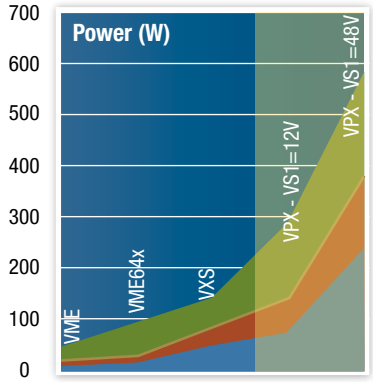

Figure 2

Compared here is the range of actual power dissipation for various embedded board technologies. The blue section represents what are considered "low power" boards; the red section represents what are considered "typical power" boards, and the green section represents what are considered "high power" boards.

and conduction-cooled products. VXS allows VME to address new applications that require additional bandwidth and higher performance than VME can support. Table 1 lists a summary of the VXS ANSI/VITA standards and draft standards. VXS is an evolution of VME, and as such it provides good backward compatibility with VME systems. VME64x modules without P0 connectors can plug into VXS slots. And VXS payload modules can plug into VME64x slots without J0.

VPX Gathering Momentum

VPX has a number of significant advantages for embedded mil/aero applications. It supports both 3U and 6U form-factors, and offers a large amount of high-speed rear I/O. Four 4x fabric links to each slot give VPX double the fabric bandwidth of VXS. And most importantly for military applications, VPX with its companion REDI standards, is designed from the ground up to support two-level maintenance.

VPX products have been in the market for less than a year, and the market is still developing. The VPX ecosystem is growing very quickly, with more than 26 COTS products announced by seven vendors. This includes air-cooled, conduction-cooled and liquid flow-through (demonstrator) products. Table 2 lists a summary of the VPX and REDI VITA standards, all of which are still in draft phase.

Thermal Challenges

High-performance switched fabric-based embedded computing industry standards are rapidly increasing in popularity. Maturing industry standards include PICMG's AdvancedTCA (ATCA) and VITA's VXS (VITA 41), as well as emerging industry standards such as PICMG's AMC and MicroTCA, and VITA's XMC (VITA 42), VPX (VITA 46) and REDI (VITA 48). These new industry standards support high power densities as

compared to mature industry standards such as CompactPCI, PMC and VME. Figure 1 depicts the thermal density in mW/cm^3 for various embedded board technologies and power levels.

For plain VME, 60W was a very hot board. But for a VXS or VPX board, that's considered very low power. Figure 2 shows the range of actual power dissipation for various embedded board technologies. Rising power dissipation levels for new technologies such as VXS and VPX create significant packaging challenges. High-performance VXS and VPX chassis in the 100 W/slot to 200 W/slot range are practical today, but require detailed thermal analysis in the design phase to ensure a robust thermal design for the specific application and payload.

An example test chassis product supporting VITA 46/VPX and VITA 48/REDI is Hybricon's line of open frame desktop test chassis (the OF-XC Series) (Figure 3). The OF-XC Series chassis has open side access for engineering and test personnel to use for debugging VPX REDI boards. Designed to the latest VITA 46.0, VITA 46.1, VITA 46.3, VITA 46.10, VITA 48.0 and VITA 48.1 draft standards, the standard hybrid mixed VME64x-VPX Backplane provides 11 slots based on VITA 48.1 VPX REDI with 1.0-inch pitch, including support for 80 mm Rear Transition Modules in both VME64x and VPX slots. Part of Hybricon's extreme cooling chassis family, the chassis has a 2 kW Power Supply and high-performance fans with 20 cfm per slot to power and cool the most demanding new VPX boards.

The OF-XC chassis are initially available with Hybricon's standard hybrid mixed VME64x-VPX switch fabric backplane. Hybricon's backplanes have been computer simulated in Hybricon's signal integrity laboratory to ensure low signal cross talk and trouble-free system operation. The enclosures are available with 2k watts of power.

Marrying Form-Factor to Application Needs

System developers now have several choices for embedded system applications. As they have done many times before, the VITA standards community has developed new standards to extend the performance of VME as well as provide

VITA Standards Feature Comparison

Standard Feature	VME64x & ANSI/ VITA 1.7 & ANSI/ VITA 31.1	VXS	VPX	
	6U	6U	6U	3U
Differential High-Speed I/O pairs	none	14 pairs	192 pairs	64 pairs
Single Ended High-Speed I/O (if all pins used)	none	31	400	120
Fabric Ports per Board	(2) 10/100/1000 Base-T	(2) 4x ports	(4) 4x ports	(4) 4x ports
Ethernet	ANSI/ VITA 31.1	GigE VITA 41.3	(planned) VITA 46.6 & VITA 46.7	(planned) VITA 46.6 & VITA 46.7
Serial RapidIO	no	VITA 41.2	VITA 46.3	VITA 46.3
PCI Express	no	VITA 41.4	VITA 46.4	VITA 46.4
InfiniBand	no	VITA 41.1	TBD	TBD
VMEbus backward compatible	yes	yes except P0	Hybrid b/p VITA 46.1	Hybrid b/p VITA 46.1
Support 2-Level maintenance	no	no	Yes VITA 48.x REDI	Yes VITA 48.x REDI
Maximum power per board	3.3V:66W 5V:90W 12V:24W -12V:24W	3.3V:66W 5V:90W 12V:24W -12V:24W	5V:120W 12V:384W or 48V:768W	3.3V:79W5V:120W 12V:192W
Liquid flow-through module cooling	no	no	yes. VITA 48.3 & VITA 48.4	yes. VITA 48.3 & VITA 48.4
Fiber optic rear I/O	no	no	planned	planned

Table 3

In this comparion of VME versus VXS and VPX, ANSI/VITA 31.1 is shown as a good choice for 6U applications that require an Ethernet switch fabric and full backward compatibility with VME. VXS provides significant performance advantages over ANSI/VITA 31.1, and it has become a popular choice for signal processing apps. VPX REDI, while still quite new, has significant performance advantages over VXS based on performance, I/O capability, two-level maintenance and 3U form-factor support.

Figure 3

Supporting VITA 46/VPX and VITA 48/REDI is Hybricon's line of open frame desktop test chassis. Called the OF-XC Series, the chassis has open side access for engineering and test personnel to use for debugging VPX REDI boards. Designed to the latest VITA 46.0, VITA 46.1, VITA 46.3, VITA 46.10, VITA 48.0 and VITA 48.1 draft standards, the standard hybrid mixed VME64x-VPX Backplane provides 11 slots based on VITA 48.1 VPX REDI with 1.0-inch pitch.

an evolutionary path for VME-based systems. Table 3 lists a detailed comparison of VME versus VXS and VPX. ANSI/VITA 31.1 is a good, low-cost choice for 6U applications that require an Ethernet switch fabric. It is fully backward compatible with VME. For applications that fit this profile, it is worth a look.

VXS provides significant performance advantages over ANSI/VITA 31.1, and it has become a popular choice for signal processing applications because of the well developed board ecosystem as well as the performance level. VXS changes the VME64x P0/J0 connector, limiting the backward compatibility with VME64x boards and backplanes that use P0/J0. That said, VXS does otherwise provide very good backward compatibility with VME. It's expected to continue to enjoy design wins for that reason alone.

Meanwhile, VPX REDI is new, but the ecosystem is developing at an explosive rate. VPX REDI has significant performance advantages over VXS based on performance, I/O capability, two-level maintenance and robust 3U form-factor support. VPX REDI has a bright future and will be widely adopted as the ecosystem develops. Several programs have already selected VPX. One thing to keep in mind with VPX is that the connectors are incompatible with VME, so backward compatibility can only be achieved with hybrid systems having a mixture of VPX slots and VME/VXS slots. When choosing a form-factor, the important point is matching it to the application. ■■

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Reconfigurable Approach Wins for Adaptive Beamforming

Using model-based design for hybrid DSP/FPGA implementations and modular, reconfigurable hardware, a complex communications system can be developed that enables adaptive multi-channel beamforming.

David Neumann, Sr Principal Engineer and
Curtis Nelson, DSP Engineer,
U.S. Navy, SPAWAR Systems Center - Charleston
Nory Nakhaee, Chief Executive Officer and
Bogdan Vacaliuc, Chief Technology Officer,
Sundance DSP

Advances in signal processing hardware are enabling the use of smart antennas and digital beamforming in communication systems for better reception and more users in the same amount of spectrum. Multi-channel digital beamforming is so computationally expensive that only reconfigurable hardware is capable of implementing it in real time.

Such systems require the coordination of large numbers of DSPs and FPGAs. A joint venture between Sundance DSP and the U.S. Navy SPAWAR Systems Center - Charleston has produced a system that enables adaptive multi-channel beamforming by utilizing closely coupled DSP/FPGA hardware. A model-based design method using the Simulink modeling tool, the PARS toolbox, and the Diamond environment and RTOS automate the translation from model to software/firmware.

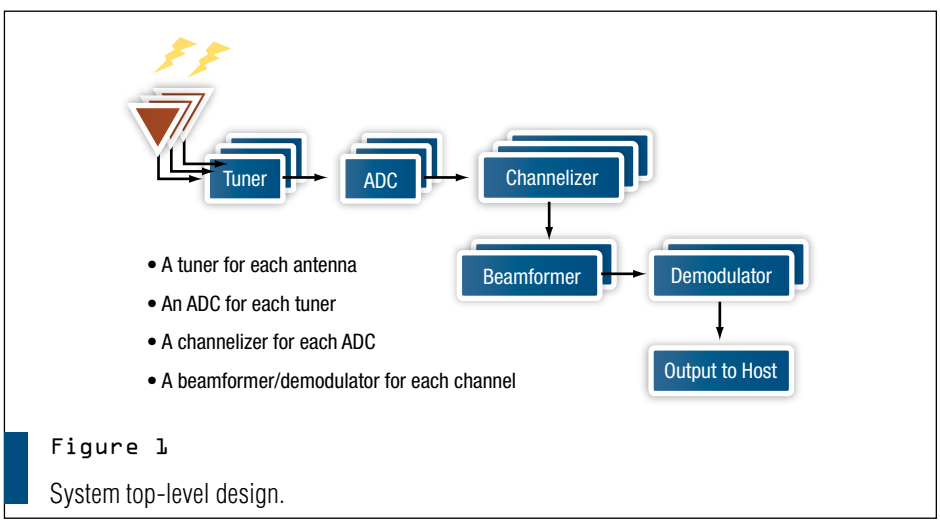

Figure 1
System top-level design.

Why Use Model-Based Design?

In a traditional communication design flow featuring embedded signal processing components, most errors are made in the research and development phases. However, most of these errors are only detected later, during the testing and integration of the system's components. Model-based design seeks to eliminate this trend.

Under the principles of model-based design, stages may be divided as follows: 1) design, 2) modeling, simulation and prototyping, 3) code generation, 4) verification, and 5) implementation and system test.

These are performed hierarchically, and with the right tools, the outer stages can be performed in parallel. This process enables each component of the system to be modeled/generated/verified continuously throughout the development cycle. As changes in the design occur, the framework already exists to immediately observe the impact it has upon the entire system.

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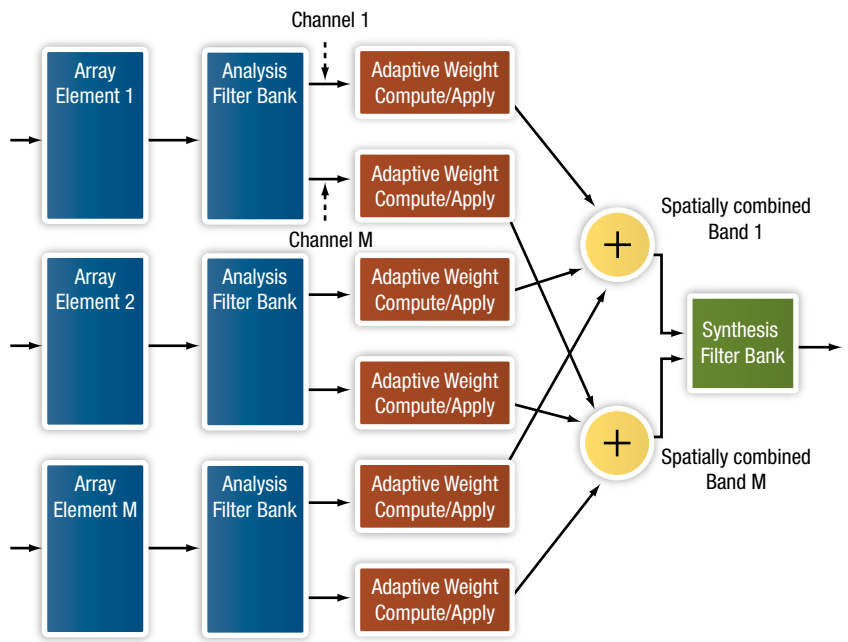

Figure 2

Beamformer processing model.

QTY	COMPONENT	DESCRIPTION
2	SMT148-FX	Quad TIM Site Carrier w/USB2.0
2	SMT364	Quad 14-bit 105MSPS ADC
2	SMT318-SX55	**Dual XC4VSX55-12 FPGA module**
2	SMT374-300	**Dual TMS320C6713-300 w/256 Mbytes SDRAM**
2	SMT361Q	**Quad TMS320C6416-600 DSP module**
1	SMT399-Fxxx	OCXO High Precision Clock module
1	Enclosure	Custom 2U Rack Mount Enclosure

Table 1

Listed here are the Sundance modules used in the beamforming system. Included are multi-channel A/D converters, a dual-FPGA card, floating-point and fixed-point DSP cards and a precision clock source.

Beamforming Background and Design

The SPAWAR Systems Center - Charleston wished to have a rapid development system capable of exploring various types of beamforming methods on a large number of channels sharing the same spectrum. As a proof-of-concept demonstration, it was decided to have several Family Radio Service (FRS) FM radios transmit on the same channel at the same time and build a system capable of processing all of their signals. The FRS narrowband FM system operates in the 462.5625 to 467.7125 MHz band with 25 KHz channel separation.

At the top-level design of the system, a linearly arranged and equally spaced array of antennas forms the basic receiving structure (Figure 1). An array of programmable tuners shifts the spectrum of interest to a 21.4 MHz intermediate frequency (IF) for digitization. By using appropriate "look" directions, the beamformed system can selectively receive from any or all of the radios without any jamming occurring between them.

Due to the requirement for a large number of channels, the channelization architecture chosen for the FPGA is a polyphase filter bank. It implements a uniformly distributed multi-channel filter using an FFT. This implementation offers greater channel capacity compared to the traditional digital down-converter (DDC) for the same size silicon space. For optimum adjacent channel rejection, SPAWAR provided Sundance a custom filter design.

The DSP section implements a space-time adaptive beamforming algorithm. Beamforming allows arrays of sensors to discriminate between signals in one direction relative to background noise and interference in other directions. The important point to note is that the signals obtained from different antennas in the array differ in phase (determined by the distance between antenna elements) as well as in amplitude (determined by the weight associated with that antenna).

The beamforming architecture uses the Minimum Variance Distortionless Response (MVDR) beamformer (Figure 2). The adaptive algorithm enables the system to receive and separate multiple transmissions on the same frequency band based on direction of arrival of the signal of interest. The system adapts to changing conditions of the environment as well as the motion of interfering transmitters in space.

The Sundance modules used in this system include multi-channel analog-to digital converters, a dual-FPGA card, floating-point and fixed-point DSP solutions and a precision clock source (Table 1). All modules were attached to a carrier card. Several Sundance FPGA IP cores and application blocks and libraries were also used to reduce development time.

Simulation

Having readily available acquisition hardware to collect real sampled data was a key factor in developing the polyphase filter coefficients.

MATLAB, from The MathWorks, was used to perform simulation and exploration of the mathematical operations of the entire process. This covered pre-filtering through the polyphase decomposition and FM demodulation. M-script is an interpretive language and results in quick visualization of any proposed implementation.

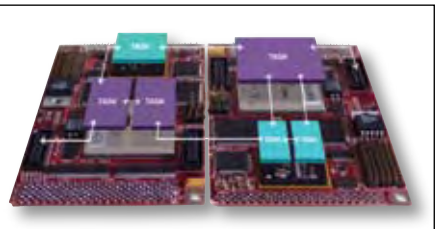

Figure 3

Task partitioning and placement onto DSP/FPGA system resources, handled automatically by the Diamond environment and RTOS.

These simulations were used to define the specifications of the various processing "blocks," as well as to clearly express to the team members what the underlying mathematics involved for each process was. Once these were defined, they could be modeled in Simulink, also from The MathWorks, quite straightforwardly.

Code Generation

The Simulink tool enables the hierarchical design and connection of processing blocks. These blocks represent the same expressions and operations of the mathematically oriented M-script, but with the emphasis on dataflow, inter-block connections and overall system architecture.

Parallel Application from Rapid Simulation (PARS) is a Sundance toolbox that allows MATLAB and Simulink users to rapidly design, simulate and generate code for a multi-DSP, multi-FPGA system. All development work is based on platform-independent models.

Diamond, from 3L, is an environment and RTOS based on communicating sequential processes. Initially targeting the transputer, it has evolved into the de facto standard OS of all Sundance DSP module implementations. Its ability to encapsulate the implementation of FPGA tasks within its process flow means that interfaces between FPGA and DSP are now completely ubiquitous and transparent. This enables closely coupled interaction between DSP and FPGA tasks.

Diamond tasks, which are derived from Simulink blocks, are mapped onto actual hardware by the Diamond configuration process (Figure 3). PARS assists in the translation by expressing the code generated by Simulink's Real-Time Embedded Coder (for DSPs),

HDL Coder (for FPGAs) or Xilinx System Generator (for FPGAs) as Diamond tasks.

Verification

"Hardware-in-the-loop" is a term used when selected parts of the model are exchanged with a data I/O system and an equivalent implementation on the target hardware. Modeling the processor and I/O constraints provides more accurate verification blocks.

In order to minimize development risk, subsystem groups of verified blocks can also be targeted for verification as part of a phased system integration plan. PARS takes advantage of the "divide-and-conquer" philosophy for large-scale development of multiple DSP/FPGA hybrid systems.

Finally, the entire system can be executed under controlled input vector conditions; result vectors are compared against the golden model executing in simulation. For every test vector input, the testbench can generate and compare a simulation/system output. Testbenches can be set to auto-generate test vectors to verify system behavior under expected as well as atypical conditions.

Deployment

Once the hardware and software tasks are qualified under this process, it becomes a simple matter to render the entire system as an embedded application.

Diamond supports this step at the lowest level by providing the technology to encapsulate the software and firmware for all the DSPs and FPGAs in the entire system into a single executable image. Loading the entire processing network is simply a matter of providing this image to the "root" device of a multi-DSP, multi-FPGA network.

Simulink bridges the gap between the mathematics and the platform-independent model. PARS bridges the gap between the Simulink model and the deployable embedded system. Diamond makes it all possible.

As wireless revenues dominate the $8.3 billion 2006 DSP market, representing 72.5% of it, rapid development and deployment methods for communications systems continue to define reconfigurable hardware as the most relevant technology driving this market. ■■

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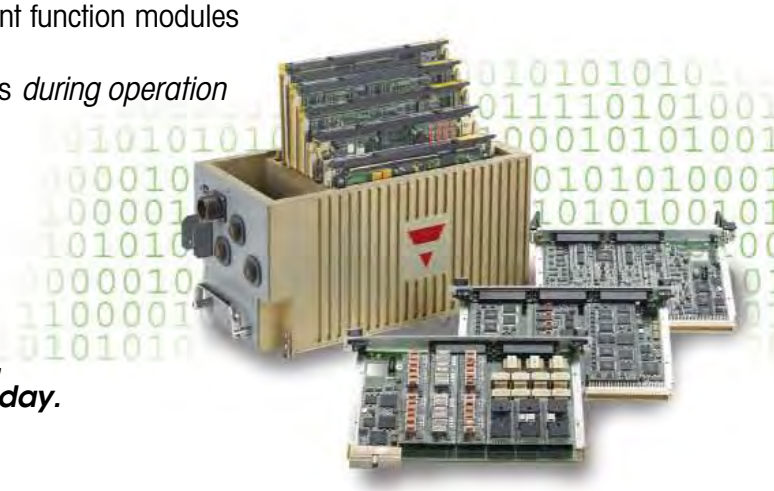

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Tech Recon

FPGAs and Reconfigurable Computing Boards

Defense Systems Make the "SWAP" to FPGAs on PCI-104

Reconfigurable computing via FPGAs and PCI-104 is satisfying the military's demand for maximum application performance, significant SWAP advantages and flexibility, in systems such as UAVs and UGVs.

Malachy Devlin, Chief Technology Officer, PhD.
Nallatech

Small form-factor signal processing solutions are becoming critical to the success of defense development efforts. Applications such as sensors and communications for Unmanned Aerial Vehicles (UAVs) and Unmanned Ground Vehicles (UGVs) have strict size, weight and power (SWAP) requirements. These applications must deliver high performance within the SWAP constraints of the target platform. PCI-104-based technologies have long met the needs of similar applications, albeit with relatively lower performance when compared to industry standard PCI-, CompactPCI- and VME-based solutions.

FPGAs can be easily molded to SWAP requirements and are becoming a significant processing technology for carrying out the computationally intensive front-end signal processing calculations, such as real-time FFT, digital down-conversion and signal detection. Originally, these devices were only conceived to be utilized as glue logic. However, with their rapid increase in capacity and performance, FPGAs have proven that they are able to carry out integer-based algorithms. In the latest device families, they now offer significant floating-point capability.

The PCI-104 form-factor can host the latest FPGA technology, which has driven high-performance FPGA computing vendors to enter this space. Within an FPGA-based PCI-104 motherboard, it is now possible to achieve maximum sustained rates of 40 GFLOPs single precision, 12.8 GFLOPs double precision and 128 Giga operations per second (GOPs) (16-bit integer in a single PCI-104 stack). When this is compared with the latest DSP processors that offer 1.4 GFLOPs peak single precision and 16 GOPs peak (16-bit integer), it illustrates the strides that FPGAs have made as processing engines in recent years.

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SIGINT Applications Need Processing Performance

A common application domain within UAVs and UGVs is signal intelligence (SIGINT) applications. Such applications require a large amount of processing performance to carry out the five stages for extracting intelligence from environmental data. These stages are raw signal, digitized data, information extraction, knowledgeable interpretation and intelligence output.

Not only can the FPGA naturally morph its silicon resources to match the optimal data types ranging from bit manipulation through integer to floating-point data, it is equally capable of directly interfacing and managing data conversion resources, such as A/D converters and D/A converters.

This level of integration enables a single device to handle the pin signaling of the data converters, read or write data from/to the data converters, carry out the heavy lifting DSP using integer arithmetic, extract meaningful data from the signals received and make intelligent decisions on this data, which may be executed with floating-point data. This system processing chain is regularly used in electronic support measures (ESMs), which are systems that typically consist of an array of

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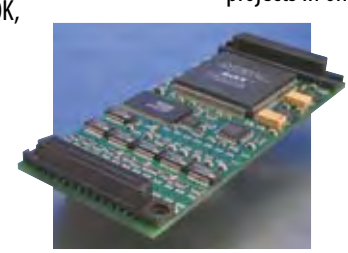

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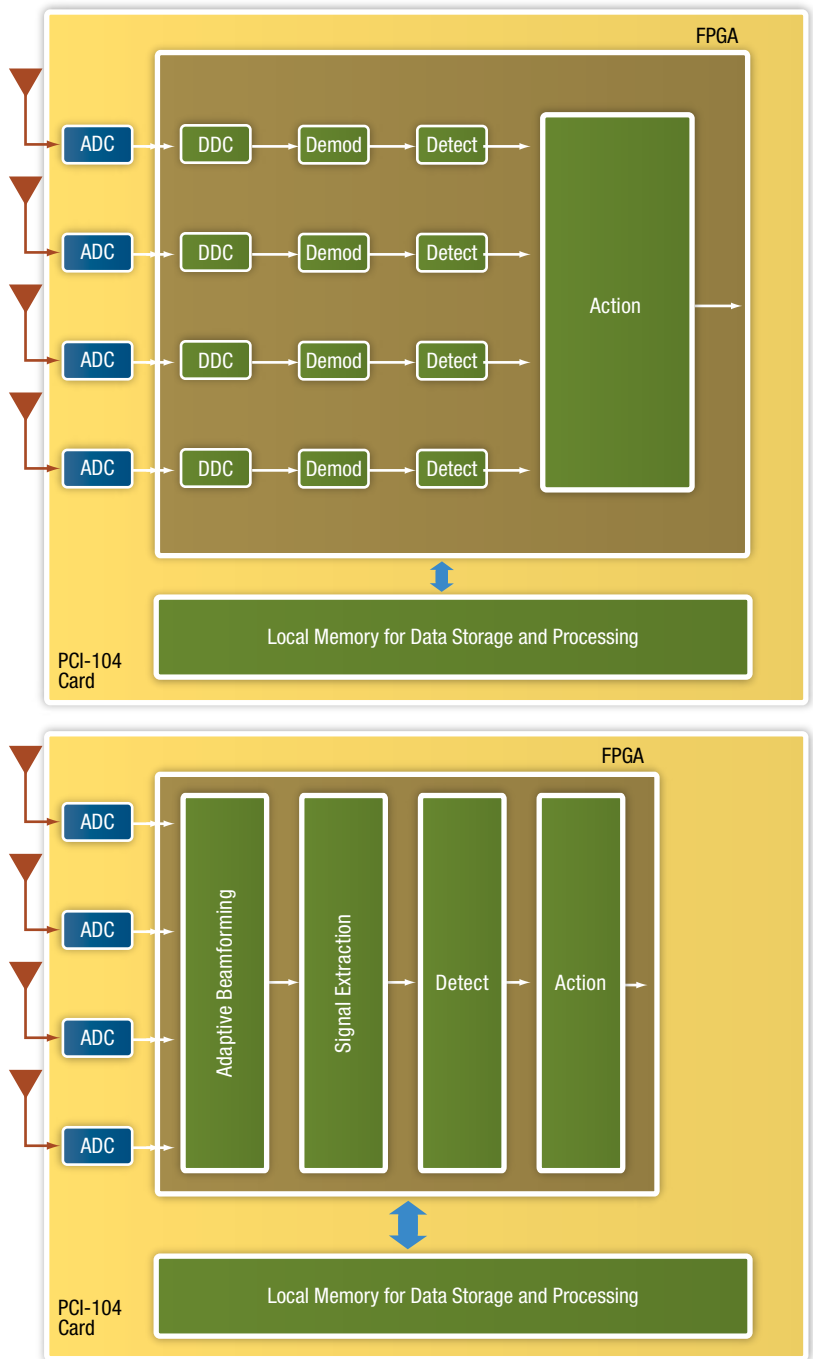

Figure 1

Example of an electronic support measure (ESM), typically an antenna array that captures signals within different frequency bands and acts upon information extracted from those bands.

sensitive antennas that capture signals within different frequency bands and act upon information extracted from these frequency bands. The FPGAs can consume the antenna data at full rate and perform the digital down-conversion, channelization and demodulation.

For example, multiple FFTs or other signal transformation can be applied to the channels for information extraction and delivered to a detection algorithm. Due to the parallel nature of the computations carried out in the FPGAs, all channels can be processed simultaneously, allowing the detection algorithms to work with the channel independently or carry out a cross-correlation on all channels.

The power of this approach enables the ESM to detect, track and respond to multiple external threats while maintaining data throughput, even if the algorithms are made more complex. By contrast, microprocessors typically require more software cycles as the algorithms get more complex, and thus the data rate or the number of channels must be reduced to match the performance of the microprocessor.

This ESM is based on the Nallatech PCI-104 system with a quad 12-bit 250 Msamples/s A/D converter directly connected to a Xilinx Virtex-4 device. In this system, data is captured from four individual antennas that are processed separately. It is only at the end of the processing chain that the detected data is combined to aid in improved accuracy of the action to be taken (Figure 1).

A second application based on this same PCI-104 system harnesses the technique of adaptive antenna arrays, in which the data from all four antennas is combined as it arrives from the data converters. By carrying out this signal processing technique directly on multiple antennas, the system can electronically steer the antennas to "look" in a particular direction to maximize the signal/noise ratio of the data received, while also acquiring an accurate direction of arrival (DoA) of the signal being

Figure 2

High-performance PCI-104 hardware can be used in harsh military environments when specially packaged, such as in the HiDANplus unique packaging system from RTD Embedded Technologies.

observed and tracked.

This optimal data is then used in the remainder of the processing chain to extract intelligent information upon which action can be taken. There are many other possibilities for systems that can be implemented with an antenna array. Their common requirement is for vast amounts of processing capability to handle 1.5 Gbyte/s of data, a manageable task that can be delivered by the FPGA. As an example, the Virtex-4 XC4VSX55 provides 512 dedicated MAC units in addition to 5.76 Mbits of dedicated internal memory and a large array of logic. This translates to dedicated DSP blocks that provide 256 Giga multiple accumulates/second (GMACs/s) and an internal memory bandwidth of 703 Gbytes/s.

FPGAs and PCI-104 Tackle SDR

The combination of computing performance with the flexibility of reconfiguring the computing engine leads to many possibilities for radio systems. Software defined radio (SDR) is a common objective of many systems as the number of different radio transmission systems expands. These radios can be reconfigured with different waveforms to enable a common hardware platform to be compatible with the widest range of radio transmissions.

A further evolution of SDR is that of cognitive radio, in which the radio system has sufficient intelligence to reconfigure itself to address the needs of the signal analysis environment within SIGINT, or the application and user demands within a communications environment. For example, upon detection of eavesdropping, a radio system could automatically switch encryption standards or move to a less

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		CMX158886PX1400HR	CMD158886PX1400HR	CMX158886PX1400HR-BRG	CMD158886PX1400HR-BRG	CME147786CX400HR	CME147786CX650HR	CML147786CX400HR	CML147786CX650HR	CMX147786CX400HR	CMX147786CX650HR	CME26686CX333HR	CME27686CX333HR	CMC26686CX333HR
Bus	AT Expansion Bus			✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	PCI Universal Expansion Bus	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	
	PCI Bus Masters	4	4	4	4	4	4	4	4	4	4		4	
	APIC (add'l PCI interrupts)	9	9	9	9	9	9	9	9	9	9			
CPU and BIOS	CPU Max Clock Rate (MHz)	1400	1400	1400	1400	400	650	400	650	400	650	333	333	333
	L2 Cache	2MB	2MB	2MB	2MB	256k	256k	256k	256k	256k	256k	16K	16k	16k
	Intel SpeedStep Technology	✓	✓	✓	✓									
	ACPI Power Mgmt	2.0	2.0	2.0	2.0	1.0	1.0	1.0	1.0	1.0	1.0			
	Max Onboard DRAM (MB)	512	512	512	512	512	512	512	512	512	512	256	256	256
	RTD Enhanced Flash BIOS	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Nonvolatile Configuration	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Quick Boot Option Installed	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	USB Boot	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			
Peripherals	Watchdog Timer & RTC	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	IDE and Floppy Controllers	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	ATA/IDE Disk Socket, 32 DIP	1	1	1	1	1	1	1	1	1	1	1	1	1
	Audio	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			
	Digital Video	LVDS	LVDS	LVDS	LVDS			TTL	TTL	LVDS	LVDS	TTL	TTL	
	Analog Video	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	
	AT Keyboard/Utility Port	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	PS/2 Mouse	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	USB Mouse/Keyboard	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
I/O	RS-232/422/485 Ports	2	1	2	1	2	2	2	2	2	2	2	2	2
	USB 2.0 Ports	2	4	2	4									
	USB Ports					2	2	2	2	2	2	2	2	2
	10/100Base-T Ethernet	1		1		1	1	1	1	1	1	1	1	
	ECP Parallel Port	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	aDIO(Advanced Digital I/O)	18	18	18	18	18	18	18	18	18	18	18	18	18
	multiPort(aDIO, ECP, FDC)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SW	ROM-DOS Installed	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	DOS, Windows, Linux	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

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Bus	AT Expansion Bus	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	PCI Expansion Bus Master	✓	✓				✓							✓	✓
	McBSP Serial Ports	✓	✓				✓								
Analog Input	Single-Ended Inputs	16	16	16	16	16	16								
	Differential Inputs	8	8		8	8	8								
	Max Throughput (kHz)	1250	1250	40	500	100	1250								
	Max Resolution (bits)	12	12	12	12	16	12								
	Input Ranges/Gains	3/7	3/7	3/1	3/4	1/4	3/6								
	Autonomous SmartCal	✓	✓												
	Data Marker Inputs	3	3		3		3								
Conversions	Channel-Gain Table	8k	8k		8k	8k	8k								
	Scan/Burst/Multi-Burst	✓	✓		✓	✓	✓								
	A/D FIFO Buffer	8k	8k		8k	8k	8k								
	Sample Counter	✓	✓		✓	✓	✓								
	DMA or PCI Bus Master	✓	✓		✓	✓	✓	✓						✓	
	SyncBus	✓	✓				✓								
Digital I/O	Total Digital I/O	16	16	16	16	16	16	16	48	18/9	32	64	32	48	48
	Bit Programmable I/O	8	8		8	8	8	8	24	6/0				48	✓‡
	Advanced Interrupts	2	2		2	2	2	2	2					2	
	Input FIFO Buffer	8k	8k		8k	8k	8k							4M	8M
	Opto-Isolated Inputs										16	48	16		
	Opto-Isolated Outputs										16	16			
	User Timer/Counters	3	3	3	2	3	3	3	3	3				10	6
	External Trigger	✓	✓		✓	✓	✓	✓	✓					✓	
	Incr. Encoder/PWM									3/9					✓‡
	Relay Outputs												16		
Analog Out	Analog Outputs	2	2		2	2	2	4							
	Max Throughput (kHz)	200	200		200	100	200	200							
	Resolution (bits)	12	12		12	16	12	12							
	Output Ranges	4	4		3	1	4	4							
	D/A FIFO Buffer	8k	8k				8k	8k							

‡ User-defined, realizable in FPGA

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	Height	49.8	35.81	71.8	93.8	115.8
Weight* (Kg)		0.3	0.343	0.473	0.686	0.899
Typical Power Consumption** (W)		25	30	40	55	70
Max # of FPGAs available		1	2	3	5	7
Max # of MSPS class ADCs		0	4	4	8	12
Max # of GSPS class ADCs		0	2	2	4	6
Single Precision Floating Point (including SBC)	Max Sustain GFLOPS	20	40	60	100	140
	GFLOPS/m3	27.5	71.0	61.7	81.9	95.4
	GFLOPS/W	0.5	0.9	1.1	1.4	1.6
	GFLOPS/Kg	44.9	82.0	97.1	120.3	134.1
Double Precision Floating Point (including SBC)	Max Sustain GFLOPS	6.4	12.8	19.2	32	44.8
	GFLOPS/m3	8.8	22.7	19.7	26.2	30.5
	GFLOPS/W	0.2	0.3	0.3	0.5	0.5
	GFLOPS/Kg	14.4	26.2	31.1	38.5	42.9
16 bit integer (including SBC)	Max Sustain GOPS	64	128	192	320	448
	GOPS/m3	88.2	227.3	197.3	262.2	305.2
	GOPS/W	1.6	2.8	3.4	4.5	5.2
	GOPS/Kg	143.8	262.3	310.7	385.1	429.1

Table 1

Scalability levels achievable with PCI-104 FPGA-based computing systems.

congested part of the spectrum.

FPGAs make possible algorithm scalability by enabling the parallelization of tasks on the silicon itself. When this is coupled with the PCI-104 platform, further orders of scalability can be achieved (Table 1). At the upper end, these PCI-104 systems can provide a level of computing performance in the space of a shoe box that previously may have required a 42-in. rack.

Furthermore, an increase in the number of channels and sampling rate of external analog I/O over traditional processor-based systems is also achieved. It is now possible to scale a PCI-104 system up to 12 channels of 12 bits at 250 Msamples/s tightly coupled with four high-end FPGAs. For maximum spectrum analysis it is also possible to create a PCI-104 system with six analog interfaces, each capturing analog data at 3 Gsamples/s. This enables a small form-factor to directly analyze over 3 GHz of spectrum instantaneously, thus covering the L band and part of the S band.

PCI-104 has proven itself in a range of applications such as "detect and avoid" imaging and target tracking. When using high-performance PCI-104 hardware in enclosed systems, special attention to cooling methods is required, since many SIGINT applications operate in hostile environments where air-cooled techniques or the use of fans are prohibited. More mechanically rugged techniques, such as conduction cooling, are required to withstand harsh shock and vibration conditions and poor internal airflow environments. One high-performance SIGINT data analysis system has been developed using RTD Embedded Technologies' HiDANplus, a unique packaging system for deployment in harsh environments (Figure 2).

In sensor and communication applications for UAVs and UGVs, military system designers and integrators face the typical engineering challenge of continually growing demand for computing performance as algorithms mature, incorporate more intelligence and require higher data rates. These requirements alone would be manageable.

However, there are also SWAP envelopes that cannot be exceeded. Fortunately, the innovative use of new technologies such as FPGAs and the adaptation of small form-factors such as PCI-104 demonstrate that these challenges can be successfully addressed and new generations of SIGINT systems can be created. The PCI-104 form-factor is a scalable option for addressing these demanding applications such as target detection and tracking, as well as for directly handling intermediate frequency (IF) radio communications. ■■

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FPGAs for Stream Processing: A Natural Choice

High-performance stream processing of incoming signal or image data needs the flexibility provided by reconfigurable computing, as well as the ability to address system-level design and cost issues provided by FPGAs.

Mark Littlefield, Product Marketing Manager, FPGA-Based Products,
Curtiss-Wright Controls Embedded Computing
Jeff Wetch, NA Business Development Manager,
Xilinx, Aerospace and Defense Division

Many military and aerospace applications require high-performance processing of incoming signal or image data streams. This I/O "stream processing" often includes filtering, conditioning, correction or decimation. Although custom ASICs are sometimes used for stream processing, they are inherently inflexible and long, expensive design cycles can make them a less than ideal solution. In addition to demanding processing requirements, stream processing applications frequently need to address system-level issues including size, weight and power (SWAP), time to deployment, field upgradeability and dynamic, on-the-fly reconfigurability.

RISC or DSP processors configured in a multicomputer based on a flexible communications fabric might seem a natural design choice for stream processing systems. However, SWAP or system cost pressures often prevent defense and aerospace developers from deploying a system comprising only RISC or DSP processors. In comparison, modern FPGAs—with their reconfigurability, large gate counts, DSP units and built-in high-speed serial ports—can provide system designers with a better alternative.

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Attributes of Stream Processing Systems

In a typical stream processing application some feedback information may pass from later to earlier stages, but the majority of data movement is in a unidirectional stream. While the earlier stages tend to be DSP-like, the later stages entail more symbolic processing. As the type of processing changes, the hardware used for each stage may also change (Table 1).

A typical stream processing multicomputer system is heterogeneous. It includes I/O boards (sensor interfaces or A/D converters), FPGA processing boards, quad-PowerPC boards for floating-point DSP and other general-purpose processing and SBCs for control and device I/O (Figure 1). The system's input devices are connected to the FPGA computing engines via dedicated serial links, and the various processing elements are interconnected via a switching communications fabric.

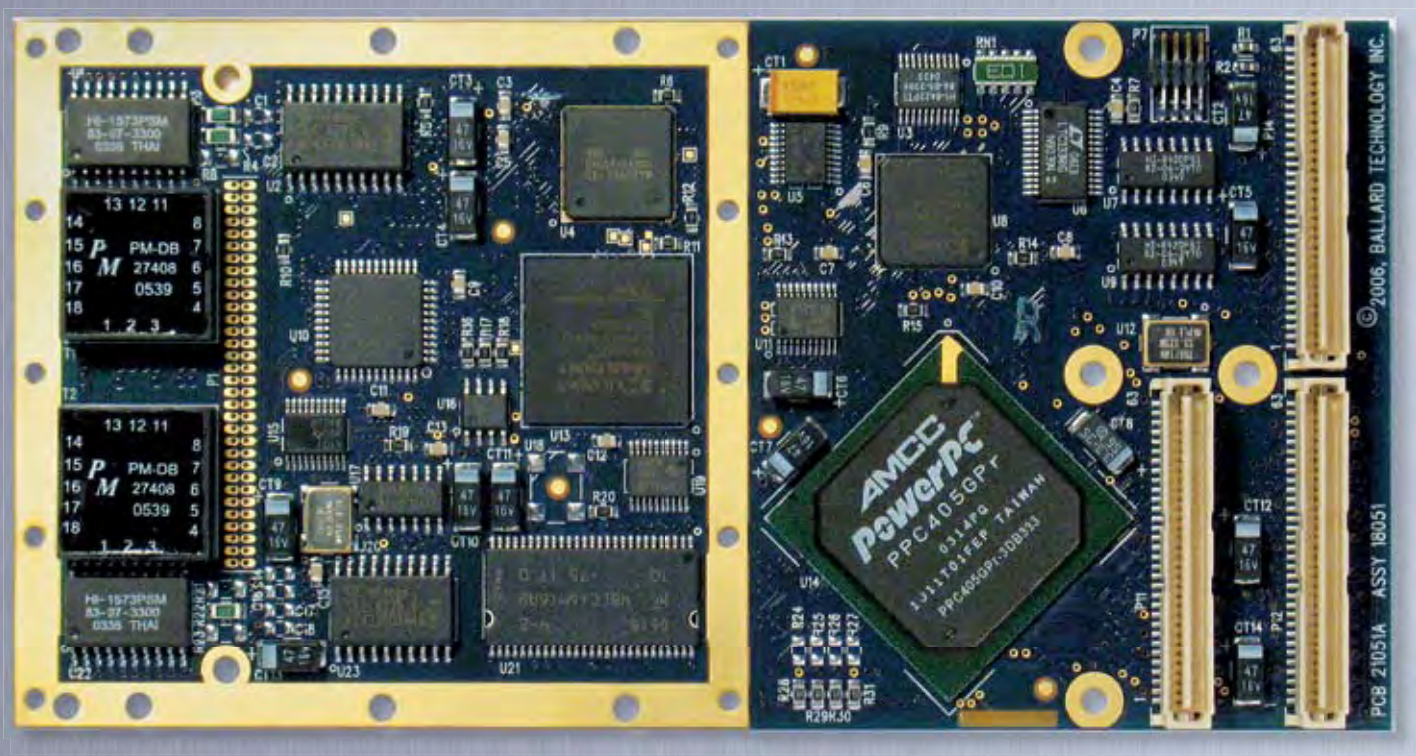
Using FPGAs for Early-Stage Processing

Modern FPGA technology is ideally suited to solving the early stage processing problem in a stream processing system. For example, the Xilinx Virtex-5 provides large gate-count logic, specialized floating-point DSP units, and high-speed serial ports in a 65 nm process package designed to minimize both leakage current and the FPGA's overall static power dissipation. The 65 nm process also reduces node capacitance, which in turn reduces dynamic power consumption in conjunction with the FPGA's 1-volt core voltage.

The device's ExpressFabric architecture has an enhanced lookup table (LUT) structure that provides six inputs to support compact designs. The DSP48E DSP blocks have 25 x 18-bit multipliers to enhance the FPGA's floating-point functionality. These blocks can be pipelined or cascaded to increase the throughput of various filtering algorithms.

The LXT version of this FPGA includes up to 24 high-speed/low-power serial I/O channels with performance from 100 Mbits/s to 3.2 Gbits/s and supports many high-speed serial I/O standards. In addition to soft cores for Aurora or RapidIO communications, it also contains dedicated hardware blocks for Gigabit Ethernet and PCI Express.

Commercial platforms for use in stream processing applications can take optimal advantage of the Virtex-5 LXT's advanced features for high-performance early-stage stream processing. For example, a dual LXT-based board's high-speed serial ports can be routed to the backplane, the mezzanine site, the Serial RapidIO (SRIO) fabric and between its two FPGAs so that four-lane links can be established between these natural I/O paths. In addition, 18 pairs (36 pins) of discrete LVDS signals can be routed from



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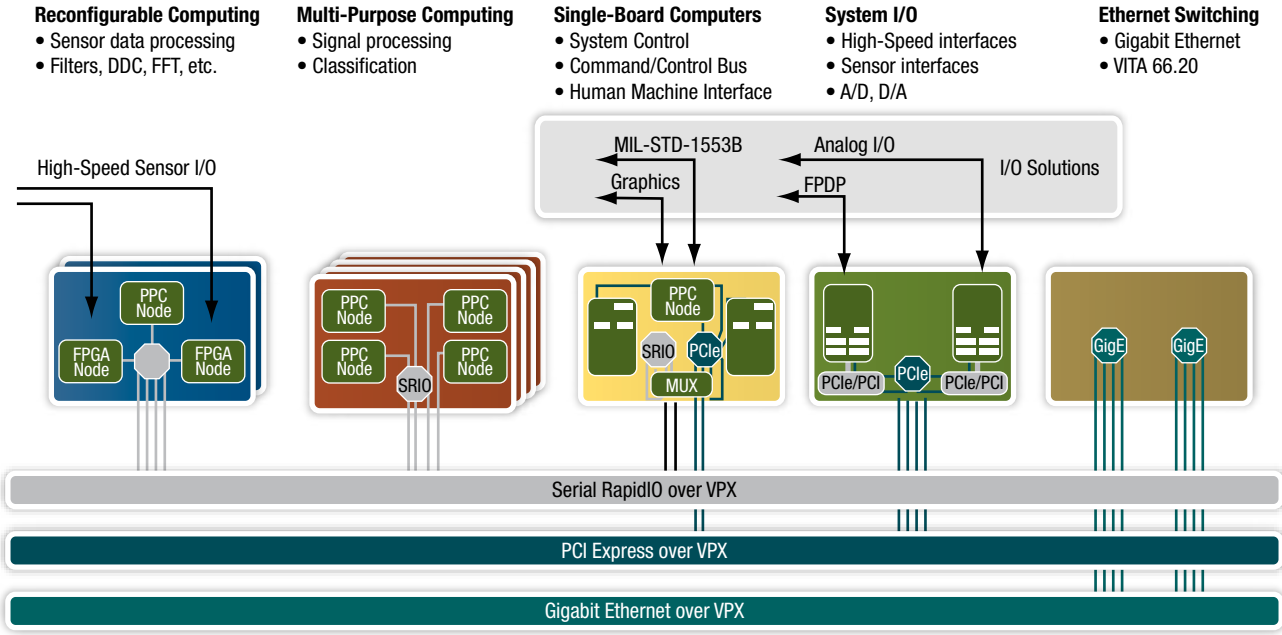

Figure 1

In a typical stream computing system, I/O and processing elements are connected by one or more connection fabrics. Here, FPGA- and PowerPC-based computing elements are linked with different I/O options via Serial RapidIO for interprocessor communications, PCI Express for I/O and Gigabit Ethernet for control.

each FPGA to the rear panel for parallel or custom I/O.

Multiple SRAM and SDRAM banks on a board can ensure that the FPGA application has adequate memory bandwidths for storing and accessing filter coefficients, temporary algorithm data, scroll buffers or historical data. When each memory bank is also multi-ported, developers have maximum flexibility for parallelizing or pipelining their FPGA designs.

Integrating FPGAs into the System

Such a board's FPGA nodes could be used to perform the calculations needed for early-stage stream processing. While the nodes are physically connected to the communications fabric and contain advanced DMA engines, they lack the flexibility of general-purpose processors (GPPs) for managing sophisticated data movements.

For example, DMA setup and control is typically handled by an external GPP node. A dual-core AltiVec-enabled Freescale 8641D Power Architecture (PowerPC) processor supports these tasks and other critical services such as FPGA configuration or rapid reconfiguration, interprocessor synchronization tasks or dynamic adjustment of calculation parameters such as filter coefficients.

Many of these tasks can be performed through the back-side control bus, which avoids disrupting data flows through the SRIO fabric. These functions are typically initiated in application code through OS or board-support package (BSP) function calls, or, increasingly, via a communications middleware layer.

The mid- and late-stage processing stages in a stream processing system are typically performed by PowerPC GPPs. In addition to handling the FPGA command-and-control tasks, an onboard PowerPC can participate in these processing stages as a peer processor to those found on quad-DSP or SBCs. These stages of processing, which often involve floating-point vector calculations, can be handled by the AltiVec unit in the 8641D. Both the onboard and off-board PowerPCs in such a system benefit from rich system and middleware software by easing the overall integration effort and by abstracting hardware details that result in better portability of application code across product generations.

An example of a rugged, commercial board designed to address the requirements of stream processing applications is Curtiss-Wright's CHAMP-FX2, a 6U VPX/VPX-REDI board that combines dual LXT FPGAs and a dual-core 8641D PowerPC processor (Figure 2).

When using such a board for stream processing, a common system model is to distribute data out from the FPGA to other processors in the multicomputer, either in a round-robin or a next-available-processor fashion. FPGA toolkits provide drivers and a software library for managing these complex data movement strategies as well as interfaces for a wide range of board-related features, including node configuration, temperature and current sensors and control bus access. They also provide elements such as IP block libraries, simulation environments, BSPs, algorithm libraries and middleware.

The Continuum FXtools toolkit for the CHAMP-FX2 provides advanced

DMA engines in several of its IP blocks. These DMA engines support round-robin or a next-available-processor data distribution either in a PowerPC-driven model, a continuous chained DMA model, or, in the case of the SRIO Endpoint block, a data-driven model. Because the setup and control of such data movements are fairly sophisticated, a GPP is often used for control.

The board is also supported with a communications middleware package, Continuum Inter-Processor Communications (IPC), which has been extended so that the FPGA-related buffers and data movements can all be managed through the relatively high-level APIs that it provides. IPC utilizes named buffer, synchronization and data movement objects to ease system integration and aid in porting to next-generation platforms for technology refresh by masking the details of the underlying hardware from the application-level code. ▮▮

Figure 2

The rugged Curtiss-Wright CHAMP-FX2 6U VPX/VPX-REDI board features dual high-performance Xilinx Virtex-5 LXT FPGAs and a dual-core Freescale 8641 PowerPC processor. Serial RapidIO (SRIO) connects three computational nodes and an onboard XMC mezzanine site with up to four 4-lane SRIO connectors to the backplane, while high-speed serial ports connect the FPGAs to each other, the XMC site and front-panel or back-panel connections.

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Task	Processing Stage	Characteristics	Processor Type
Signal conditioning, filtering, digital down conversion, sensor correction, backprojection	Early	Fixed-point, some floating-point	FPGA, Fixed-Point DSP
Beamforming, image convolution	Early/Mid	Fixed or Float	FPGA, Fixed-Point DSP, PowerPC, x86
Image convolution	Early/Mid	Fixed or Float	FPGA, Fixed-Point DSP, PowerPC, x86
SAR image formation, image segmentation, moving target indication, target tracking	Mid	Floating Point	PowerPC, x86, Floating-Point DSP
Target classification	Mid/Late	Symbolic	PowerPC, x86
Sensor control, user interface	Late		PowerPC, x86

Table 1

Attributes of the types of processing stages typically found in stream processing systems.

Tech Recon

FPGAs and Reconfigurable Computing Boards

FPGAs Take Aim at Military SWAP Challenges

Design issues centered around size, weight and power (SWAP) are affecting a wide range of military programs. The current crop of FPGA technologies is helping ease those hurdles.

Charlie Jenkins, Senior Technical Marketing Manager
Altera

The military community is transforming the battlefield of the 21st century around network-centric warfare. From satellite to soldier, system size, weight and power (SWAP) are critical. Whether in manned ships, aircraft and vehicles or unmanned systems such as missiles, sensors, UAVs and UGVs, secure wireless communications are central to the solution. Further still, to cover these multiple battlefield scenarios, add the processing complexity of triple-play—voice, video and data—capabilities and multi-megabit bandwidths, and the design challenges for secure communication devices are overwhelming.

Figure 1

The JTRS HMS family of radios consists of several different variants, each designed for a different set of platforms. Shown here is the two channel Manpack form-factor.

SWAP Military Applications

Demand for secure communication use ranges across the spectrum of military systems, each with a different level of SWAP sensitivity. These range from low-sensitivity SWAP radar and airborne equipment to high-sensitivity handheld radios and sensors. Most radar and airborne systems are generally function-critical rather than SWAP-critical, having sufficient envelopes for size and power. Wireless communications within UAV and UGV systems are SWAP-sensitive, but require only a small portion of the overall power budget necessary for air and ground mobility. Munitions and missiles have extremely tight space constraints, but power sensitivity is low due to their short mission life after activation.

While airborne and maritime software defined radios have functional and heat dissipation (cooling) challenges, the most demanding requirements for SWAP applications are in handheld, Manpack (Figure 1) and small form-factor (HMS) battery-operated systems—soldiers need to carry more ammunition and body armor, not batteries. Additionally, radio form-factors, with stringent operating and

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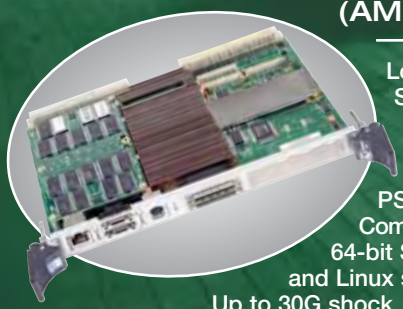

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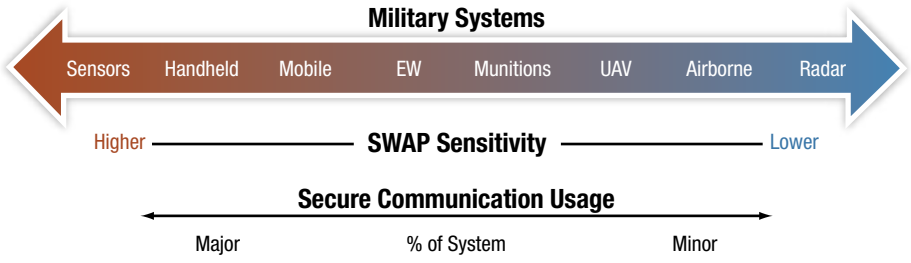

Figure 2

Military systems vary in their sensitivity to size, weight and power (SWAP) concerns. The range goes from low-sensitivity SWAP radar and airborne equipment to high-sensitivity handheld radios and sensors. Shown here is the spectrum of SWAP sensitivity over the range of various military system types.

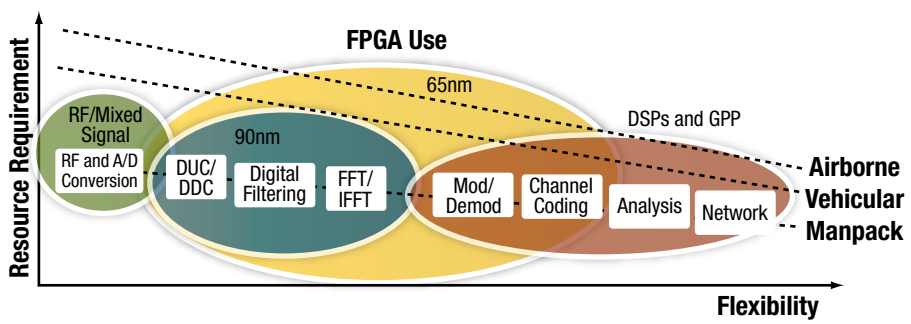

Figure 3

While 90 nm generation devices provided the right combination of resources to implement system development and demonstration radios (SDD programs), the newest 65 nm devices are optimized for lower-power and higher-functionality production applications.

deployment requirements across various battlefield scenarios, demand the smallest implementation size using a limited number of components. Figure 2 shows the spectrum of SWAP sensitivity over the range of various military system types.

Secure Communications Example

Military software defined radios (SDR) are now entering their production phases after years of feasibility, development and demonstration implementations. Advanced waveforms for SDR require flexibility and functionality beyond low-power digital signal processing (DSP) devices. New SDR designs require programmable FPGA capabilities for advanced waveforms (processing intermediate frequency (IF), modulation and bit-level functions at megabits per second), triple-play packet processing and military software communications architecture (SCA) middleware (for hardware independence), all of which push the boundaries of FPGA resources. Ultimately, the power consumption of the SDR electronics adversely affects mission life in battery-operated devices or may surpass equipment cooling requirements in extreme environments. Table 1 highlights the SWAP design challenges for battery-operated SDR.

Previous attempts to meet SDR requirements for production units have fallen short. Waveform requirements, such as variations of the soldier radio waveform (SRW), are too power-sensitive for high-performance FPGAs, but beyond the capabilities of low-power DSP devices and low-cost FPGAs. As data rates move from Kbits/s to Mbits/s, low-power DSP devices no longer have the functionality for IF, modulation and bit-level processing. Some low-cost FPGAs need multiple devices to implement the required functionality and thus limit integration capability for reducing size and weight.

Suppliers of high-performance FPGAs have tried to exploit features like voltage scaling and partial reconfiguration (for waveform integration) with little success, often causing delays in development and adding increased system risk. Without careful control of device design and manufacturing constraints, voltage scaling—lowering the voltage during radio standby conditions to reduce FPGA leakage power—can degrade verification and susceptibility of functional, timing and I/O parameters. Partial reconfiguration (the ability to reprogram portions of the FPGA while other functionality continues) for power reduction is ineffective in a high-performance, high-power process FPGA device—the unused functional areas can draw more than a watt of leakage (static) power during radio standby operation, a significant portion of time—remember the 10:1 standby to operating ratio.

Designer Goals for Success

Designers face severe functional and schedule challenges to meet SWAP program requirements. These include enabling small form-factor, lightweight military solutions; achieving waveform integration under 1W, to extend mission life and flexibility; and providing optimum value for high-volume SDR-based systems.

With these competing demands, how will designers confidently meet SWAP requirements for tomorrow's military deployments? Building on 90 nm FPGA implementations for airborne and maritime use—such as UAV, UGV, data link, munitions, electronic warfare— forthcoming power-optimized 65 nm FPGA silicon and development tool sets will create the most efficient battery-operated solutions, suitable for production to achieve the next level of design success.

New 65 nm FPGAs have the right combination of advanced architecture capabilities, coupled with the most aggressive power reduction techniques. While prior 90 nm generation devices provided the right combination of resources to implement system development and demonstra-

SWAP Design Challenges for Battery-Operated SDR

Severe size and weight restrictions.	The smallest implementations are less than 10 in^3.
Power consumption directly affects mission life	Using typical military batteries, today's programmable electronics consume over 4 watts and yield only a six-hour mission life for the overall radio system.
Power budgets dominated by digital electronic processing	As waveform bandwidth and complexity increases, digital processing absorbs more functionality and power within the radio.
Digital logic implementation trade-offs	Choices for digital processing vary from CPUs to ASICs. Typically, DSP devices and FPGAs have provided the best combination of functionality and flexibility, but suffer power trade-offs.
Static versus dynamic power trade-offs	Due to the duty cycle of radio modes, standby operation typically dominates radio use by a factor of 10:1. It is therefore imperative to minimize leakage power of digital electronics during standby operation.
Voltage and frequency scaling trade-offs to save power	With careful system design, both voltage and frequency can be scaled back in standby states, leaving only limited functionality in standby.
Software and hardware partitioning for power	Software designers need to leverage radio operational modes and intelligently manage hardware resources to effectively minimize power use.

Table 1

Listed here are the critical size, weight and power (SWAP) design challenges inherent in Software Defined Radio development.

tion radios (SDD programs), the newest 65 nm devices are optimized for lower-power and higher-functionality production applications. Figure 3 illustrates this expansion of capability and flexibility.

To enable small form-factor, lightweight SDR solutions, FPGAs capable of advanced waveform integration, with power consumption under 1 watt are available. This capability extends mission life over four times that of current implementations. To most efficiently utilize extended periods of radio standby operation, look for FPGA components with the lowest static power that enable longer battery life. SDR solutions using low-power FPGAs can use smaller, lighter and less expensive batteries, power supplies and form-factor enclosures. Soldiers will thank you. Let's examine the key developments.

FPGA Solutions

The newest 65 nm FPGAs, like Altera's Cyclone III family, are optimized for SWAP production. The combination of resource capacity (logic elements, embedded memory, multipliers and I/O) coupled with the most aggressive power reduction techniques and smallest packaging, enable superior SWAP implementations. Low-power Cyclone FPGAs are optimized for battery-operated radios with sufficient signal processing resources for advanced waveforms at 1/10th the static power compared to 90 nm devices.

The newest high-performance, high-density Stratix III FPGA family, provides maximum functionality, uses minimum power while utilizing advanced architecture capabilities including Programmable Power Technology and voltage scaling. With the maximum digital signal processing performance available, these devices are designed to address the broadest range of airborne and ground mobile radios—AMF, GMR, Manpack, Special Operation modems— as well as high-performance radar and missile systems.

Productivity tools play a key role in reducing design effort and minimizing program risk for military systems. Designers can leverage third-party and FPGA vendor IP (intellectual property) and tool offerings that accelerate time-to-

market with advanced tool capabilities—including accurate power estimation/optimization, virtual team/project management, automated system integration, and application acceleration capabilities for automating and simplifying design flow used to integrate both existing and newly developed algorithms.

High-productivity software suites that simplify porting and debugging of advanced waveforms and enable design methodologies like software programmable reconfiguration (SPR) are available. SPR methodology reduces risk and leverages IP reuse, as well as enables lower power and cost implementations using FPGA-based structured ASIC devices, such as Altera's HardCopy. It's also important to be sure that ASIC devices meet ITAR (International Traffic in Arms Regulations) guidelines, since most of these devices are fabricated in foreign semiconductor manufacturing foundries.

Supplier Ecosystem

To begin development of application software earlier, designers can leverage modular development baseboards for the desired device families. Device baseboards with high-speed I/O interfaces can extend functionality and I/O flexibility, providing advanced prototyping capabilities using modular supplier and third-party-developed daughter cards. For ruggedized system implementations, embedded board vendors offer a wide range of industry standard interface boards, including VME, PCI and AMC form-factors. Building and maintaining third-party relationships with system integrators and SCA suppliers who can provide middleware, engineering and application expertise across SDR and other military segments is essential.

Beyond SWAP solutions, it's important to evaluate FPGA suppliers on their ability to meet the special requirements of the military and aerospace market. Such capabilities include services tailored to military government contractors such as device encryption security features for anti-tampering, bare die for multichip module integration, single-event upset (SEU) detection, availability of reliable leaded packaging, and more.

Devices for SWAP applications should be qualified across industrial and military temperature ranges, including verified performance under environmental extremes. Using enhanced devices for defense applications also enables major price and life-cycle advantages, compared to dedicated military devices. A new generation of FPGAs provides the optimum solution for SWAP. FPGAs continue to offer more flexibility and functionality at reduced costs by enabling new SWAP systems with smaller footprints, lighter weight and smaller batteries. ▮▮

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System Development

MILS and Information Assurance

Information Assurance Takes Center Stage in RTOS Realm

Demand for high levels of safety and security in military systems is making MILS and Common Criteria evaluation part of the new embedded software landscape.

Rob Hoffman,
V.P. and General Manager, Aerospace and Defense
Wind River Systems

There is a growing need for multilevel secure systems in a range of aerospace and defense applications—particularly those that must be built with a high assurance of controlled security, safety, cost and schedule risk. Providing trusted data and sharing secure information have become critical for warfighters in preventing mission compromise, for homeland security in thwarting terrorist attacks, and for first responders in improving readiness for emergencies.

The problem that needs to be addressed is this: With current technologies, multilevel secure platforms and communications networks simply aren't viable. While multilevel secure systems can process information according to precisely defined security policies enforced for very high assurance, this has traditionally meant building systems with multiple physically separated hardware elements. These systems traditionally have required separate computers, separate areas on an FPGA, separate displays, or separate networks, all requiring expensive equipment and operational procedures.

The Need for Secure and Safe RTOSs

Recognizing that technological advances and threats have drastically changed the way we think about protecting our communications and communications systems, the U.S. Government has issued policies governing the acquisition of IA products for DoD Programs, called the National Security Telecommunications and Information Systems Security Policy (NSTISSP No. 11). Since July 2002, all commercial IA products must be evaluated, validated and certified in accordance with

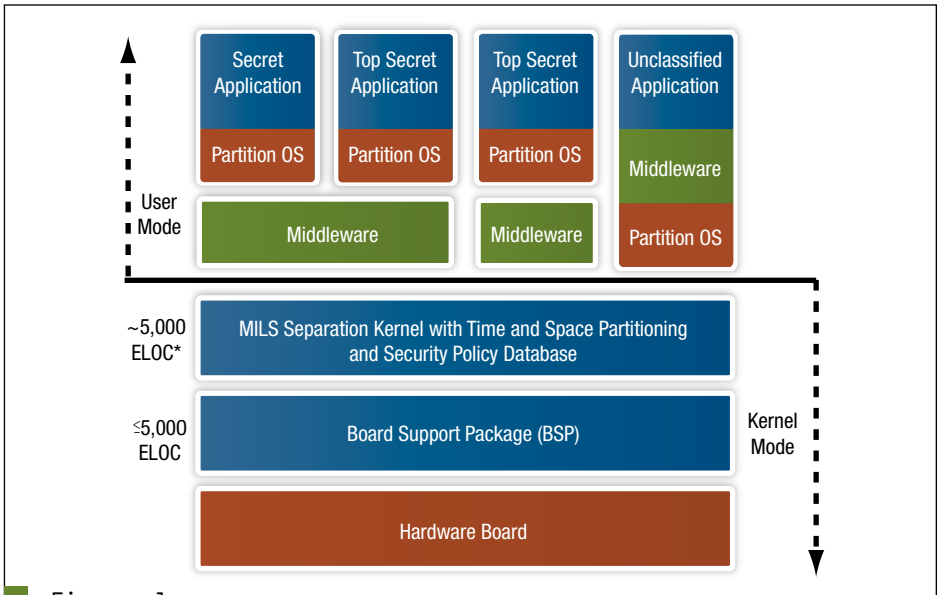

Figure 1

VxWorks MILS family of platforms, including operating systems and tools combined with middleware, comprehensive customer education, support and services. It is designed to maintain consistent, deterministic system performance, whether the need is for a few partitions or dozens of partitions to create and implement a system.

the Common Criteria for Information Technology Security Evaluation by accredited commercial laboratories. That means these multilevel systems must meet the appropriate Evaluation Assurance Level (EAL). For critical multilevel systems, the requirement is EAL6+.

MILS is an architecture that makes development, accreditation and deployment of multilevel-capable systems more practical, achievable and affordable. It can significantly increase protection, reduce development time, and reduce schedule risk of deploying technology to provide high-assurance systems that are both safe and secure. Although MILS was created in the 1980s, technology in our industry had not advanced enough to take advantage of it until recently—and to date, a high-performance system implementation does not exist.

Wind River and others are developing solutions in this area that provide a layered software architecture—real-time operating system, middleware, applica-

Figure 2

The VxWorks MILS family is based on the VxWorks ARINC 653 RTOS. The Wind River ARINC 653 RTOS is used throughout several aircraft programs including the C-130 AMP. A specially modified C-130 Hercules is shown taking off from Lackland Air Force Base. The Hercules was modified under the C-130 Avionics Modernization Program, which included a comprehensive upgrade of the avionics system.

tions and communications—that, when combined with an appropriately rigorous certification process, enable developers to create multilevel secure systems.

Yet a MILS real-time operating system (RTOS) base alone does not guarantee that a system is multilevel secure. Further, neither MILS nor Common Criteria certification guarantee that a system is functionally suitable, has adequate performance, or will achieve acceptable lifetime total cost of ownership. Overall system architecture, as well as the properties of middleware, applications and communications, must all meet security requirements and have adequate performance. But MILS, based on commercial products built using open standards, can make the development, certification, accreditation and ownership of high-assurance multilevel secure systems more achievable and affordable.

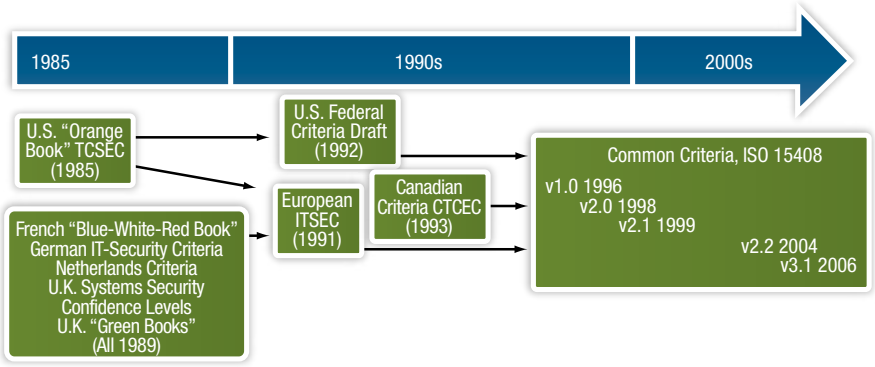

Figure 3

Illustrated here is the history of Common Criteria and its predecessors, including its relationship to the original Trusted Computer Systems Evaluation Criteria (TCSEC), the U.S. "Orange Book."

A MILS Implementation

To meet this demand, Wind River is developing the VxWorks MILS family of platforms, including operating systems and tools combined with middleware, comprehensive customer education, support and services. VxWorks MILS (Figure 1) maintains consistent, deterministic system performance, whether the need is for a few partitions or dozens of partitions to create and implement a system.

The Wind River MILS family includes the operating system "separation

kernel", secure middleware facility, and an optional Wind River Trusted Stack, all designed to meet the highest level of Common Criteria certification; and PCSexpress from Wind River partner Objective Interface Systems, a complement to the trusted stack that enables secure intrasystem and intersystem communications. To accelerate time-to-market for developers building devices with VxWorks MILS, Wind River also offers the Eclipse-based Wind River Workbench development suite. This connection to Wind River platforms provides developers with a common interface for all phases of MILS development, debug, and test. Wind River's VxWorks MILS family is based on its VxWorks ARINC 653 RTOS. The Wind River ARINC 653 RTOS is used throughout the Boeing 787 Dreamliner, the C-130 AMP (Figure 2), the Boeing 767 Tanker, and other aircraft.

Wind River's VxWorks MILSPlatforms

Wind River's VxWorks MILS Platform provides a full implementation of the MILS architecture. It enables developers to define the system architecture and to port or develop drivers, middleware, applications, and system security configurations, and it includes the required services for installation, training, and best-use consultation. VxWorks MILS will conform to the latest Separation Kernel Protection Profile (SKPP) as it evolves under the Common Criteria. While the SKPP is not yet final, changes are expected to be minor, and users can begin Common Criteria evaluation now by writing the "Security Target", documenting the "Target of Evaluation", developing the formal representations of the security requirements and functional specification, and other tasks required for high-EAL evaluation.Another key MILS tool is PCSexpress from Objective Interface Systems. PCSexpress is high-performance, real-time communications software from Wind River partner Objective Interface Systems that provides securely separated communications channels between systems. With PCSexpress, developers can easily create high-performance, GIG-connected cross-domain solutions that implement cryptography specified in the NSA's Suite B, and which are suitable for certification under Common Criteria EAL6+, DCID 6/3 PL 5, DO-178B Level A and FIPS 140-2.

As a complement to a trusted stack, PCSexpress enables secure intersystem communications and strong node / application authentication over a wide variety of communication protocols, including point-to-point—TCP, UDP, SCTP, RapidIO, InfiniBand, VME, PCI—and point-to- multipoint—IP Multicast, FireWire, USB, Link16.

The Road to EAL Common Criteria Eval

What does it take to build a real-time system suitable for high-EAL Common Criteria evaluation? Simply put, it can take several years. But even after investing years of hard engineering time and effort, high-EAL certification does not guarantee adequate functionality or performance. Today, there are no high-performance, multilevel secure systems based on the MILS architecture and a commercial operating system.

It's important to understand what the Common Criteria entails. Common Criteria (CC) for Information Technology Security Evaluation, ISO/IEC 15408, is an international standard that enables IT users to specify security requirements for products while enabling vendors to make security claims for products. It uses accredited commercial laboratories to evaluate products to determine if they meet the claims. Certification authorities in each country examine, approve and certify the evaluation. Common Criteria is the latest development of security policies for information systems. Figure 3 shows the history and the relationship to Trusted Computer Systems Evaluation Criteria (TCSEC), the U.S. "Orange Book."

The CC was developed by the governments of Canada, France, Germany, the Netherlands, the U.K. and the U.S. The National Information Assurance Partnership (NIAP), a U.S. Government initiative of the National Security Agency (NSA) and the National Institutes of Standards and Technology

EAL	Definition	Requirements	Functional Specification	HLD	Covert Channel Analysis
EAL 1	Functionally tested	Informal	Informal	Informal	No
EAL 2	Structurally tested	Informal	Informal	Informal	No
EAL 3	Methodically tested and checked	Informal	Informal	Informal	No
EAL 4	Methodically designed, tested and reviewed	Informal	Informal	Informal	Obvious vulnerabilities
EAL 5	Semiformally designed and tested	Formal	Semiformal	Semiformal	moderate attack potential
EAL 6	Semiformally verified, designed, and tested	Formal	Formal	Semiformal	Systematic
EAL 7	Formally verified, designed, and tested	Formal	Formal	Formal	Systematic

Table 1

Each representation at the different EAL level is either specified formally using a mathematical notation, semiformally using a structured natural language, or informally. Rules are provided that require "proof" of the equivalence of adjacent representations, with the required "proof" a function of the type of representation—formal, semiformal, or informal. The requirements at the different levels are shown here.

(NIST), administer the Common Criteria in the United States. NIAP maintains a Web site for the Common Criteria Evaluation and Validation Scheme at http://niap.bahialab.com/cc-scheme.

Evaluation Under Common Criteria

Common Criteria uses an Evaluation Assurance Level (EAL) to define each increasingly rigorous package of assurance requirements. Each numbered package, from EAL1 through the highest level, EAL7, represents a point on the CC's predefined assurance scale. An EAL can be considered a level of confidence in the security functions of an IT product or system. Products evaluated to EAL1 through EAL4 are mutually accepted by each of the 24 participating countries under the Common Criteria Recognition Agreement, while critical systems processing national security information must be evaluated at EAL5 or higher, in the U.S. by the NIAP Evaluation and Validation Program. For cryptographic products, the NIST Federal Information Processing Standards (FIPS) validation program is used.

The successive evaluation levels define increasing rigor for five representations of the particular IS system to be evaluated: the security requirements model, functional specification, high-level design, detailed or low-level design, and implementation. Each representation at the different EAL level is either specified formally using a mathematical notation, semiformally using a structured natural language, or informally. Rules are provided that require "proof" of the equivalence of adjacent representations, with the required "proof" a function of the type of representation—formal, semiformal, or informal. For example, at EAL7, both the security model and functional specification must be specified formally and their equivalent proved mathematically. The requirements at the different levels are shown in Table 1.

Testing Labs Responsible for Evaluations

Under NIAP, NIST is responsible for accrediting evaluators. Nine evaluators are accredited. These are called Common Criteria Testing Labs in the U.S. The NSA is the Validation Body and is responsible for certifying all evaluations as well as the in-depth covert channel penetration testing at EAL6 and EAL7. The Common Criteria evaluation process is based on several key concepts. Of particular importance is the joint cooperation between customer and OS vendor for development of the following:

Protection Profile (PP): An implementation-independent set of security functional and assurance requirements for a category of IT products that meet specific consumer needs. The latest list of approximately 60 types of protection profiles is available at www.commoncriteriaportal.org.

Security Target (ST): A set of security functional and assurance requirements and specifications to be used as the basis for evaluation of an identified product or system (the security claims often made by reference to specific PPs).

Target of Evaluation (TOE): The IT product or system described in a PP or, more typically at high EAL, an ST. The TOE is the entity subject to security evaluation.

An early step in the development and certification of a multilevel secure system to high EAL is to determine which Protection Profiles are applicable, then develop drafts of the Security Target (the security claims) and the Target of Evaluation (system description) documentation for review by the NSA. ▮▮

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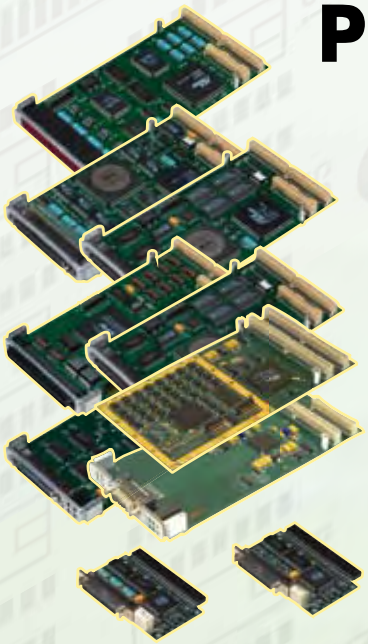
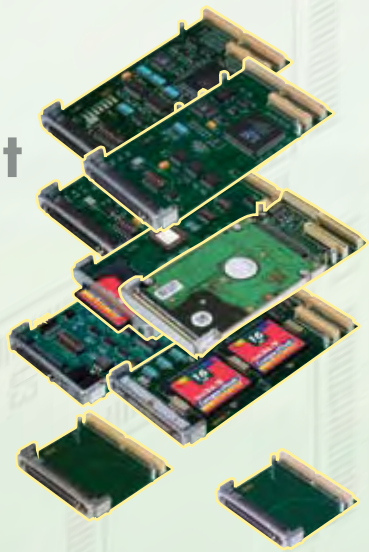


Serial

Ultra320

FPGA

Quad Ethernet



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SCSI

Async

SATA

Reconfigurable

RoHS

CardBus

IDE

Digital I/O

CompactFlash

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PrPMC

SAS

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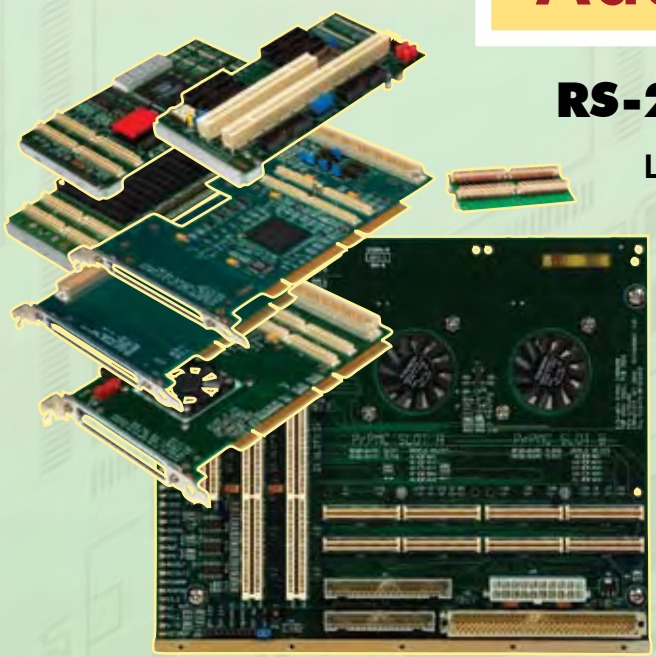

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Military Test Systems Take Flight on PXI, VXI and LXI Boards

PXI, VXI and now LXI boards are being used to test complex, sophisticated, high-performance military systems.

Ann R. Thryft
Senior Editor

As military systems become increasingly sophisticated and complex, their successful development depends even more on powerful test and instrumentation equipment. Just as the designers of those systems and subsystems are basing them on commercial board-level components, so the equipment used to test them is also being built out of standard and embedded computers. As a result, the days when military system designers had to make their own custom measurement instruments are long gone. Instead, a rich set of high-performance instruments is available off the shelf for almost any need in a wide variety of applications, such as radar, electronic warfare, satellite and military communications (Figure 1).

Two open specifications, PXI and VXI, have arisen to serve these needs. Each has a rich, established ecosystem of board products and design options.

Courtesy of U.S. Air Force.

Figure 1

PXI, VXI and increasingly LXI boards are being used as test platforms for testing sophisticated, complex military systems during their development phase. In particular, systems and subsystems aimed at aircraft must withstand a barrage of testing by heavy-duty test and instrumentation equipment. The F-22 Raptor's aerodynamic design, advanced flight controls, thrust vectoring and high thrust-to-weight ratio allow it to outmaneuver its adversaries.

For example, modular test architectures such as PXI (PCI eXtensions for Instrumentation) let designers craft synthetic instrumentation systems that can replace standard digital multimeters, oscilloscopes, power meters and frequency counters in RF and microwave test systems. PXI, which has become an industry standard for measurement applications, combines standard PC technology with integrated timing and triggering to deliver a platform with up to 10 times performance improvement over older architectures.

As a spin-off from CompactPCI, the PXI form-factor defines a rugged, CompactPCI-based platform that has been optimized for test, measurement and control applications, which can leverage the critical mass and existing ecosystems already achieved by CompactPCI. The PXI Systems Alliance, originators of the specification, boasts more than 68 member companies, and more than 1,150 PXI products are currently available. A variation of PXI is PXI Express. By utilizing PCI Express as a bus, PXIe opens up multiple, higher-bandwidth design possibilities for military test and measurement and data acquisition applications.

The VXIbus, the competing VME-based specification, is PXI's older cousin. It was developed by extending the VME bus standard to better accommodate instruments. This includes the addition of power supply voltages, analog and triggering buses, as well as power, cooling and EMC specifications for modules, and C- and D-sized modules for larger layouts. Standard instrument VXI products are available from over 80 vendors and the platform can accept PXI, VME and M-Module cards.

A third standard, the emerging Ethernet-based LXI specification for automated test systems, is also becoming popular in military test and instrumentation projects. Introduced in 2005, LXI (LAN eXtensions for Instrumentation) defines small instruments using low-cost, open-standard LAN (Ethernet) as the system backbone. It reduces the time needed to set up, configure and debug test systems. LXI's compact, flexible package, high-speed I/O and use of Ethernet meet the needs of aerospace and defense engineers developing a wide variety of systems. Military engineers can leverage the software and measurement accuracy they currently have from their GPIB instruments to an LXI-based test system. The LXI Consortium boasts 44 member companies and organizations. ▮▮

LXI Consortium
[www.lxistandard.org].

PXI Systems Alliance
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Modular test architectures such as PXI let military system designers create synthetic instrumentation systems that can replace a host of traditional digital equipment. ADLINK is smoothing the way with its latest high-speed, high-resolution, high-capacity PXI digitizer, the PXI-9820 data acquisition card. Equipped with 14-bit resolution, 30 MHz of bandwidth and single- or dual-channel sampling rates of up to

130 Msamples/s and 65 Msamples/s, respectively, the PXI-9820 is engineered for high-level signal acquisition applications such as military radar and ultrasonic, digital broadcasting. It is equipped with two analog inputs and two synchronous digital inputs (SDIs). Input ranges of -1 volt to 1V or -5V to 5V are selected via software, and input impedance is selected through solder points. 128 Mbytes of RAM, expandable to 512 Mbytes of standard SODIMM SDRAM records several seconds of data at single-channel sampling rates.

Analog triggering can be configured through numerous options, and digital triggering supports rising-edge and falling-edge triggering. The PXI-9820 also implements PXI star trigger and PXI trigger bus to route timing and trigger signals between one or more PXI-9820s and other PXI modules. Either the internal clock, the output of the onboard PLL with a reference clock from an external clock input, or the PXI 10 MHz reference clock can be used to synchronize multiple PXI modules in a system. The PXI-9820's two SDIs allow digital input to be synchronously sampled with analog input, making it suitable for mixed-signal acquisition. Auto-calibration adjusts the gain and offset to a specified accuracy, eliminating the need to manually calibrate modules. Pricing for boards in the PXI-9820 series ranges from $3,950 to $4,150.

ADLINK Technology America
Irvine, CA.
(949) 727-2077.
[www.adlinktech.com].

Arbitrary Waveform Generator Is Class A LXI-Certified

LXI is the next-generation, Ethernet LAN-based modular architecture standard for automated test systems managed by the LXI Consortium. It is catching on fast among military designers, which is not surprising considering the military's growing affection for Ethernet. Helping to build out the product offerings in the nascent LXI architecture, Agilent Technologies has announced six microwave synthetic instruments that are the industry's first Class A LXI products to be certified by the LXI Consortium. They support the DoD's NxTest vision of flexible, modular and compact instrumentation. One module in the series, the N8241A, is an arbitrary waveform generator featuring simultaneous 1.25 Gsamples/s sampling and 15-bit resolution, enabling military designers to create ideal waveforms for accurate test of radar, satellite, digital radio and frequency agile systems. It offers dual-channel, single-ended, differential outputs with 500 MHz of instantaneous analog bandwidth per channel.

Synthetic instruments link hardware and

software modules to emulate standard test instruments in a compact form-factor, resulting in a common system architecture that enables DoD prime contractors to design scalable, morphable automated test systems that can accommodate new measurement applications and future technology updates. Each channel of the N8241A arbitrary waveform generator module provides either 500 MHz of modulation bandwidth (for the 1.25 GHz sampling rate), or 250 MHz of modulation bandwidth (for the 625 MHz sampling rate). With over 65 dBc of spurious free dynamic range, very high-fidelity complex modulation signals can be generated. When the N8241A is combined with a wideband I/Q upconverter, modulation bandwidth of 1 GHz (for the 1.25 Gsample/s sampling rate) or 500 MHz (for the 625 MHz sampling rate) can be realized at microwave frequencies for authentic signal simulations for IF and RF subsystem test. Depending upon capabilities, pricing for the N8241A ranges from $33,570 to $84,160.

Agilent Technologies
Palo Alto, CA.
650) 752-5000.
[www.agilent.com].

PXI Express Data Capture Card Boasts 600 Mbytes/s Sustained

Data capture and playback is essential to military PXI users for high-performance measurement and automation. The PXI Express standard creates an ultra-fast environment for these functions by increasing controller-to-backplane bandwidth. It also broadens

the application set for PXI data acquisition. Conduant's new StreamStor PXIe-416 high-speed, real-time data recording system supports PXI Express products for exponential performance improvements over older instrumentation measurement and automation architectures. Applications include high-speed image acquisition, as well as recording RF signals in the field for later playback and analysis in a lab. The 3U PXIe card has four-lane endpoint connectivity to the host PXI Express fabric and can record at 600 Mbytes/s sustained for more than 3 1/2 hrs. The card supports more than 8 terabytes of storage attached as four separate StreamStor DM4 data modules with a total of sixteen 500 Gbyte disk drives.

The StreamStor PXIe-416 records and/or plays back as peer-to-peer transfers within the PXI-Express fabric, eliminating contention with non-real-time elements of the computer system. It is compatible with the standard StreamStor API and software utilities. Additional features include simultaneous recording and playback; simultaneous recording of streams from multiple data sources within the PXIe fabric by a single StreamStor data recorder; simultaneous playback of recorded data to multiple destinations in the PXIe fabric from a single StreamStor data recorder; and event marking via the PXI Real-Time System Integration bus (RTSI). Bundled pricing for board, storage chassis and drives starts at under $12,000.

Conduant
Longmont, CO.
(303) 485-2721.
[www.conduant.com].

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3U PXI Boards Serve Up Digital I/O Feast

Complex automatic test requirements are far from rare in the military world. Feeding that need, the GX5292 series of high-performance, cost-effective 3U PXI dynamic digital I/O boards from Geotest have 32 TTL input or output channels and 32 LVDS input or output channels. The GX5292 series can address a variety of high-performance digital test needs, including real-time recording and playback for digital video and digital IF applications. It expands on the company's GX5280 series by incorporating dynamic direction control on a per-pin and per-vector basis. The GX5292 also supports deep pattern memory by offering 256 Mbytes of onboard vector memory with dynamic per-pin direction control and test rates of up to 100 MHz. The single-board design supports both master and slave functionality without the use of add-on modules.

The GX5292 supports selectable I/O levels of 1.5V, 1.8V, 2.5V, or 3.3V (TTL, LVTTL, CMOS, LVCMOS), in addition to 32 differential channels for LVDS, M-LVDS, or LVDM logic families. The TTL/LVTTL interface utilizes a programmable voltage source that sets output logic levels from 1.4V to 3.6V. Programmable thresholds of 1.5V, 1.8V, 2.5V, or 3.3V (5V-compatible) are supported for input signals. Recommended operating input voltage range is from 0V to 5.5V. Required PCI memory space for each board is only 16 Mbytes, preserving

test system resources. A direct mode is also supported for continuous data transfers. The GX5292 offers 256 Mbytes of vector memory, with 64 Mbits per channel. Vector memory can be software configured to support channel widths of 32, 16, 8, 4, 2 and 1 with corresponding vector depths of 64 Mbits, 128 Mbits, 256 Mbits, 512 Mbits, 1,024 Mbits and 2,048 Mbits. Pricing ranges from $4,995 to $5,994.

Geotest-Marvin Test Systems
Irvine, CA.
(949) 263-2222.
[www.geotestinc.com].

Board Duo Sports 100% Performance Improvement

Designed specifically for modular instrumentation and data acquisition applications, the new Intel Core 2 Duo-based family of PXI and PXI Express embedded controllers from National Instruments delivers performance improvement of more than 100% compared to systems running traditional single-core processors. Based on the 2.16 GHz dual-core Intel Core 2 Duo processor T7400, the NI PXI-8106 and NI PXIe-8106 controllers integrate seamlessly with multitasking environments and multithreaded applications. They deliver a performance improvement of up to 46% for applications based on National Instruments' LabVIEW graphical development platform, compared to systems using Intel's Core Duo dual-core architecture. With the widely used SYSmark PC benchmarking software, the controllers demonstrate an overall performance improvement of 29% compared to

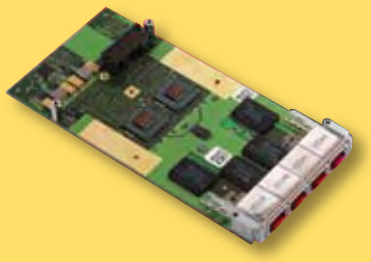
previous-generation dual-core controllers and 67% compared to previous-generation single-core controllers.

Gigabit Ethernet is featured for high-speed networking in distributed systems. The integrated ExpressCard slot gives engineers the choice of additional peripheral I/O, such as external RAID hard drive arrays for high-speed streaming to disk. The controllers also feature a Serial ATA hard drive, DVI-I digital and analog video and additional I/O such as high-speed USB, GPIB, serial and parallel ports. An extended temperature, extended operation hard drive is optional for applications that include high and low temperature extremes or require 24/7 operation. Both Windows XP Professional and LabVIEW Real-Time are supported. The controllers work with a variety of NI software including LabVIEW, the LabVIEW Real-Time Module, LabWindows/CVI software for ANSI C development and NI TestStand test management software. Pricing starts at $4,499.

National Instruments
Austin, TX.
(512) 683-0100.
[www.ni.com].

XMC Extension Card Features Quad Redundant Gigabit Ethernet

As the military's use of PCI Express technology grows, there's an increasing demand for ruggedized modules that can be deployed in harsh environments. One of the first XMC extension cards for high-performance embedded military computing is the quad redundant Gigabit Ethernet P601 card from MEN Micro. Suitable for any XMC-compliant SBC or host carrier board using most bus systems, including CompactPCI, PXI and VME, it can also be used on any type of stand-alone SBC. The P601 features four high-speed Gigabit



Ethernet channels and a redundancy mode, and can be used as an extension for Windows- and Linux-based systems with multiple and ultra-fast communication requirements.

Two Ethernet controllers, connected by two x4 PCIe links, support the P601's four 10/100/1000Base-T Ethernet channels, which provide up to 1 Gbyte/s per channel in each direction. The two lines inside each controller can be configured as a redundant channel pair, where one line monitors the other and the controller can recognize when an error occurs. The new XMC card features four RJ45 connectors on the front panel as well as a passive heat sink. Options include conformal coating for protection from humid and dusty environments. Pricing is $659.

MEN Micro
Lago Vista, TX.
(512) 267-8883.
[www.menmicro.com].

Synchro/Resolver Processor Card Boasts 0.005° Accuracy

Synchro/resolver converters are electromechanical transducers designed to convert mechanical angles to electrical signals. Combined with analog and digital I/O, they provide a complete system solution for fire control systems and radar position tracking. An instrument-grade, high-density, DSP-based VXI card from North Atlantic Industries incorporates up to four synchro/resolver instrument measurement channels, up to four synchro/resolver instrument stimulus channels or up to eight synchro/resolver converter-grade stimulus channels, and up to six programmable

reference supplies. The 65CS4 C-size VXI card is a full-function instrument that performs most synchro/resolver evaluation, calibration and test functions. All functions are independent and user-programmable for either synchro or resolver format and can be formatted for single- or multi-speed applications. The unit's internal wrap-around self-test function does not require external hardware or software. Synchro/resolver measurement and instrument stimulus accuracy is to within 0.005°. Converter-grade stimulus accuracy is 0.015° loaded and 0.008° without load. Instrument stimulus and reference outputs provide 2.2 VA of drive and are programmable from 47 Hz to 4,000 Hz.

The 65CS4's stimulus channels can be programmed for continuous rotation up to 13.6 RPS or for specific start and stop angles. Measurement channels can track signals up to 4.68 RPS. Stimulus and measurement channels can be programmed for speed ratios of 2:1 through 255:1. Measurement channels provide both digital and DC angle-rate output signals. Operating temperature range is 0° to +50°C. The card provides a VXI data rate of 2 Mbytes/s, dynamic address configuration and 100 microsecond data processing. Its power supply requirement is +5 VDC at 8A (no load). Pricing for 100 pieces starts at $10,000.

North Atlantic Industries
Bohemia, NY.
(631) 567-1100.
[www.naii.com].

48 VDC Supply Provides Power for Both PXI and VXI

Few board-level products work equally well with both PXI and VXI systems. An exception to that rule is the DH-226 power supply from Tracewell Systems, which is designed to provide power for both PXI and VXI applications. Eight independently regulated outputs deliver full-rated current to meet those power requirements. Maximum output is 1,488 watts at 45°C with 400 lfm of air and typical efficiency is 90%. A special 12 VDC output is provided to operate system fans. Each output is independently thermally protected, and multiple supplies can be combined in a system with full load sharing. In keeping with the best of modern distributed power architectures, the power supply operates from a 48 VDC system bus, which is especially useful in high-power applications. The unit's high efficiency makes it ideal for portable or battery-powered applications, and also allows it to be cooled entirely by system air. The DH-226 is the size of a standard VXI card at 6U high by 7 hp wide, and weighs 6 lbs.

Front-panel LED status indicators are INPUT OK, OUTPUT OK and POWER SUPPLY FAIL. RS-485 communications allow remote monitoring of the status, internal and remote temperature sensors, external fan speed and output voltages of the power supply. Also standard is an open-collector system reset

output, which can also function as a "power good" signal. The power supply has been tested in a system to 50g's random vibration, and has been HALT tested at 1 kW load from -30° to +80°C. Pricing for the DH-226 VXI/PXI Power Supply starts at $2,670 for a minimum quantity 10 units.

Tracewell Systems
Westerville, OH.
(614) 846-6175.
[www.tracewellsystems.com].

High-Precision Digital Storage Oscilloscopes Feature 4 Gsamples/s

The PXI and VXI instrumentation architectures let engineers integrate tools such as digital storage oscilloscopes into test systems. With that in mind, ZTEC Instruments has debuted a new line of modular digital storage oscilloscopes in PXI, CompactPCI/PXI and VXI form-factors. The ZT4610 family is available in both 16 and 64 Msample/s

versions and combines an intuitive and high-speed software interface to satisfy even the most demanding automated test applications with traditional instrument ease of use for intuitive stand-alone user interaction. The mid-performance modular oscilloscope family offers a 4 Gsample/s real-time sampling rate with 800 MHz analog bandwidth. For higher acquisition rates, either equivalent-time mode (multi-capture reconstruction) or interpolated-time mode (single-capture reconstruction) can be used to achieve up to 200 Gsamples/s. Other acquisition modes include waveform averaging, high resolution and envelope detection. All multiple-capture modes allow the acquisition of up to 64k waveforms.

The 16 or 64 Msamples/s record length options provide the deep memory required to acquire and visualize even the most complex signals. Up to 32k waveforms can be rapidly captured and stored for viewing and analysis. In addition to acquisition waveform memory, four 32 kS nonvolatile reference channels and four 512 kS calculation channels are also provided. Traditional oscilloscope features, such as flexible signal conditioning, advanced triggering, auto-configuration and self-calibration, are included. The ZT4610 family includes both two- and four-channel versions. Pricing for the ZT4610 PXI starts at $7,995.

ZTEC Instruments
Albuquerque, NM.
(505) 342-0132.
[www.ztec-inc.com].

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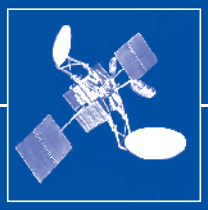

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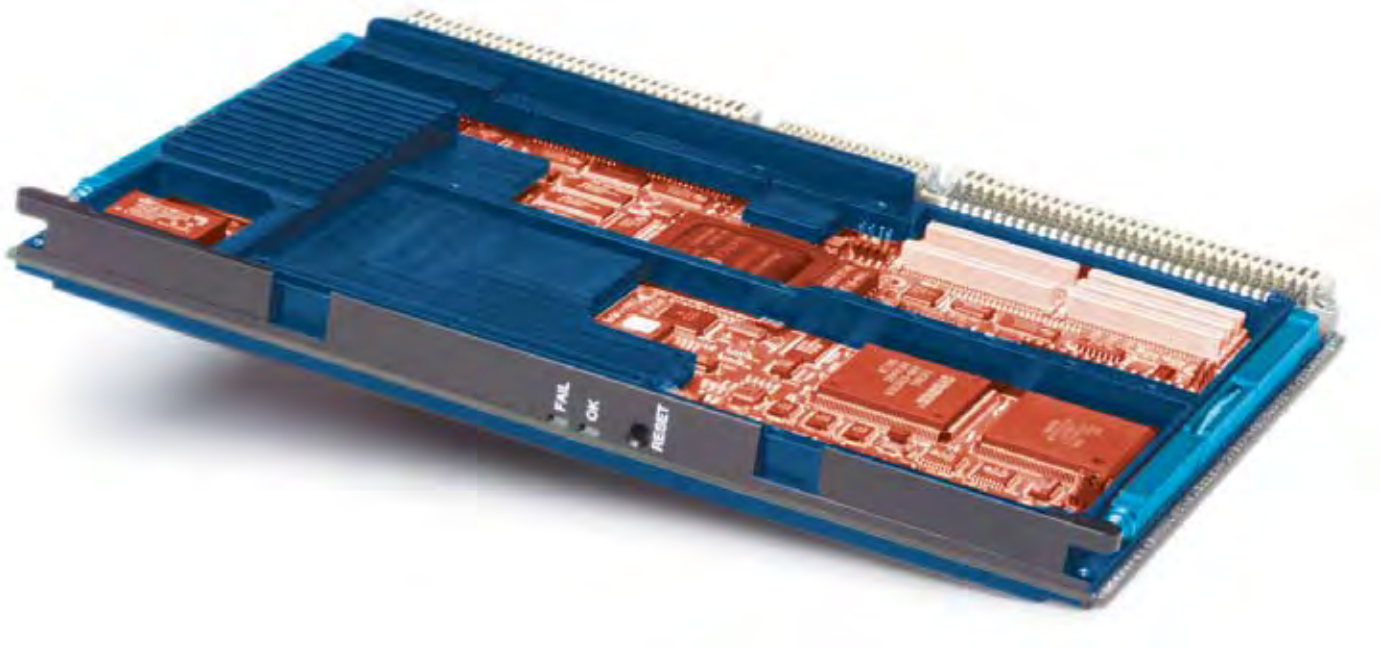

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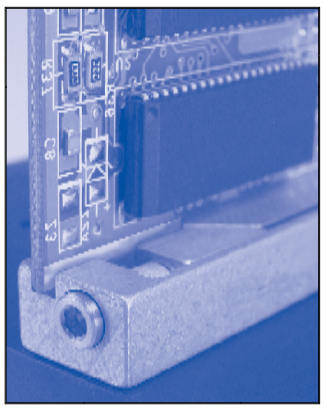

- Designed to comply with MIL-STD-810D and MIL-STD-901D in addition to MIL-E-5400

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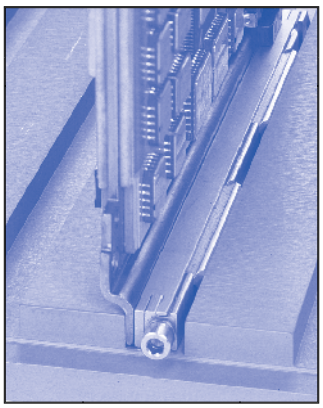

- Meets the requirements of drawing 84103, Defense Supply Center, Columbus

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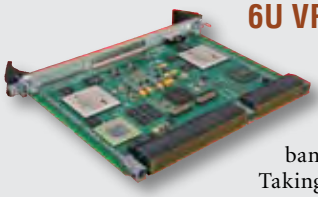
6U VPX-REDI Board Blends FPGAs and PowerPC



This could pan out to be the year of VPX. Several board vendors are planning to roll out VPX boards this year. Early to game, Curtiss-Wright Controls Embedded Computing has announced the availability of the CHAMP-FX2, its first FPGA-based VPX-REDI (VITA 46/48) compute engine. The new 6U board combines the flexibility of Xilinx FPGA-based reconfigurable computing, high performance Power Architecture (PowerPC) processing, and the high bandwidth of serial switched fabrics.

Taking full advantage of the VPX standard's support for high-bandwidth serial switched fabrics, the CHAMP-FX2 uses Serial RapidIO to connect its three computational nodes and its onboard XMC mezzanine site with up to four 4-lane SRIO connectors to the backplane. The board's memory support includes double data rate (DDR2) SDRAMs and quad data rate (QDR-II+) SRAMs that complement inter-node bandwidth by providing multiple, independent memory banks for each of the dual Virtex-5 FPGAs. High-speed serial ports are provided to connect the FPGAs to each other, to the XMC site, and to front-panel or back-panel connections. The CHAMP-FX2 is designed to operate in rugged environments and is available in both air- and conduction-cooled formats. Volume pricing for commercial and rugged versions of the CHAMP-FX2 is available.

Curtiss-Wright Controls, Embedded Computing, Dayton, OH. (937) 252-5601. [www.cwcembedded.com].

Mini DC/DC Converters Feature 300V Inputs

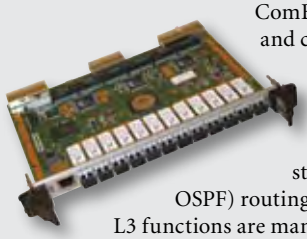
Despite their earlier reluctance, military system designers have begun to embrace the distributed power concept. It's really unavoidable in today's mixed voltage landscape. Expanding its family of mid-power Mini DC/DC converters with 300 VDC inputs, Vicor has added a 100W model at 2 and 3.3 Vout and 150W models at 5, 12, 15, 24, 28, 36 and 48 Vout. The modules incorporate Vicor's patented low-noise Zero-Current and Zero-Voltage Switching (ZCS/ZVS). Low-noise ZCS/ZVS greatly reduces the design effort and filtering costs required for power converters to meet agency conducted emissions requirements.

The converters operate from a 300V nominal input, with an input range of 180V to 375V. Efficiencies range up to 89% for the higher output voltages. These models are available in five different environmental grades, with six different pin options and three baseplate options. The modules, which are optionally available in RoHS-compliant models, are a compact 2.28 x 2.2 x 0.5 inches (57.9 x 55.9 x 12.7 mm) in size with a height above board of 0.43 inches (10.9 mm). Pricing for the 300 VDC Mini models begins from as low as $87— 5V, 150W, E Grade—in 100-piece quantities.

Vicor, Andover, MA. (978) 749-8359. [www.vicorpower.com].

GbE Switch Complies with PICMG 2.16 and VITA 31.1

Ethernet's popularity among military decision makers continues to grow. No other networking technology can boast Ethernet's longevity and wide adoption. Fueling that trend, Interface Concept has announced the ComEth4020a, a line of 6U cPCI/VME full Giga Ethernet Switches that are PICMG 2.16 and VITA 31.1 compliant, for embedded applications. ComEth4020a is built on the latest generation of Gigabit switch engine and PHY transceiver. ComEth4020a supports full-wire speed L2 bridging and L3 forwarding with L2-L4 advanced traffic classification, filtering and prioritization.



ComEth4020a switches are full managed and can easily be monitored from a browser, a remote application, a console or SNMP. The Switchware software provides layer 3 functions, allowing local IP forwarding (IPv4 / IPv6), static and dynamic protocols (RIP, OSPF) routing, proxy-ARP and DHCP-relay. These L3 functions are managed through a CLI interface. The IP routing and the L3 protocols are carried out by the processor and the forwarding is carried out by a full-wire speed L3 router. These switches can be used in all types of environments with operating ranges from standard, extended, rugged and conduction-cooled grades—operating in extended-temperature ranges of -40° to +75°C. Prices start at $6,700.

Interface Concept, Briec de l'Odet, France. +33 (0) 298 577 176. [www.interfaceconcept.com].

Rugged 6U CompactPCI Board Supports Core2 Duo

The latest crop of dual core processors offers a mix of performance for next-gen applications, while lowering the dissipated heat—an important fact when deployed in restricted space or other harsh environments. Marrying the Intel Core Duo processor to a conduction-cooled 6U CompactPCI platform, GE Fanuc Embedded Systems announced the CT11, CP11 and CR11 6U CompactPCI CPU boards. Versions are available with the Core2 Duo processor, the Core Duo processor and the Celeron M processor.

All three are designed to operate in a temperature range of -40° to +75°C (depending on configured options), with the CR11 providing option as a rugged version with stiffener bars and wedge locks or in conduction-cooled form. All three boards are PICMG 2.1 compliant for hot-swap capability. The CR11 rugged single board computer provides a unique feature set, including 4 Gbytes of soldered DDR2 SDRAM with enhanced ECC for increased reliability; two Gbit Ethernet ports; flash drive or local UDMA100 2.5-inch hard disk. Intel's IPMI interface is supported on the CT11. The CP11 delivers the same feature set as the CT11, but is a dual slot version.

GE Fanuc Embedded Systems, Albuquerque, NM. (505) 875-0600. [www.sbs.com].

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Fanless PC/104-Plus SBC Runs -40° to +85°C

Using a fan as a method of cooling an embedded board doesn't fly in military applications. Fans are too fragile to risk as the single point of failure for a system. WinSystems has introduced their PPM-GX, a PC/104-Plus-compatible single board computer (SBC) that operates throughout the temperature range of -40° to +85°C without the need for a fan. It is based upon the low-power, high-integration AMD GX500 1W processor. This SBC integrates the CPU, video, Ethernet, USB, COM, LPT, mouse, audio and keyboard controllers onto one board, yet it measures only 3.6 x 3.8 inches (90 mm x 96 mm).

The PPM-GX supports up to 512 Mbytes of SDRAM. The PPM-GX also offers support for both rotational and solid-state disks. Two floppy disk drives and two UltraDMA 66 IDE drives can be connected. Plus, there is a socket for a CompactFlash card, which can support up to an 8 Gbyte device. This solid-state disk solution is a viable alternative for fragile floppy and/or hard disk drives for use with harsh environmental applications. The PPM-GX draws typically 1.5A at +5V—which is about 8W—during normal operation. List price for the board is $495.

WinSystems, Arlington, TX. (817) 274-7553. [www.winsystems.com].

PCI Express Boards Sport Quad-Core Xeon

This is shaping up to be the year of multicore processors. And embedded board vendors have wasted no time designing such processors into board-level solutions for defense and industrial applications. Along such lines, Trenton Technology has rolled out its new MCX/MCG system host boards with dual multicore processors. MCX-series SHBs are server-class boards that provide multiple PCI Express links to option card slots and devices on a PICMG 1.3 backplane. The MCG series offers graphics-class board configurations with native electrical support for x16 PCI Express video and imaging cards.

The Trenton MCX and MCG series of system host boards provides various dual-core and quad-core Intel Xeon processor options. The dual-core options provide four execution cores on a dual-processor MCX or MCG. The Quad-Core Intel Xeon Processor E5335 option provides up to eight high-performance cores per MCX or MCG system host board. The MCX/MCG system host boards support up to 32 Gbytes of system memory. Other MCX/MCG board features include six SATA/300 interfaces with RAID support, seven USB 2.0 connections, three 10/100/1000Base-T Ethernet ports, onboard video and connection to an optional I/O expansion board for legacy I/O support. All products are available now. Typical prices range from $2.595 to $2,825.

Trenton Technology, Atlanta, GA. (770) 287-3100. [www.TrentonTechnology.com].

Four-Axis Stepper Motor Control Card Rides PCI

Top priority for today's military motor control systems is the drive toward smaller, high-precision motors and more of them. Feeding such needs, Adlink has introduced the PCI-8144, a cost-effective 4-axis stepper motor control card with four pulse output channels. The PCI-8144 delivers high-frequency pulse rates of up to 2.4 MHz, supporting high-speed motors at higher resolutions with faster acceleration. Up to 12 PCI-8144 control cards can be configured to control up to 48 axes from a single host system. The PCI-8144 also offers precise synchronization across all axes to ensure simultaneous starts and stops for accurate motion of complex systems.

The PCI-8144 supports both T-curve and S-curve speed profiles, as well as unsymmetrical acceleration and deceleration to fit a variety of applications that require fast control with smooth motion. A hardware-based emergency stop control is provided to halt the transmission of pulse trains during an emergency. The PCI-8144 also features a software security mechanism to protect your motion control applications. Software drivers for Windows and Adlink's intuitive motion control utility, MotionCreatorPro, are included to allow convenient and efficient testing and debugging of tasks.

Adlink Technology, Irvine, CA.
(949) 727-2077. [www.adlinktech.com].

VXS Board Serves Up Seven D/A Channels

Engineers developing advanced signal generation solutions for antenna array systems in applications—such as radar, electronic warfare and mobile communications—have an endless appetite for signal processing capability. Feeding such needs, TEK Microsystems has announced the new Janus VXS, the first VXS product to combine FPGA-based DSP processing technology with seven channels of 16-bit, 500 Msamples/s D/A conversion. Janus VXS is the first implementation of TEK Microsystems' new front-end / back-end modular architecture developed for its 6U VXS products. This architecture places the FPGA processing functionality on a base card, keeping the D/A and A/D processing capabilities on a mezzanine card for improved signal integrity.

The digital to analog converters are linked into a Xilinx FPGA equipped with an advanced double data rate SDRAM memory architecture with a capacity of up to 5 Gbytes on a single card. The FPGA also supports high-speed off-board communications through two front-panel, high -peed serial ports or eight high-speed links over the VXS standard P0 connector onto the backplane using protocols such as Gigabit Ethernet, VITA 55 / Aurora, SRIO, SFPDP, etc., programmable via firmware. Available now, pricing for the Janus VXS starts at $19,900 for single unit quantities.

TEK Microsystems, Chelmsford, MA. [www.tekmicro.com].

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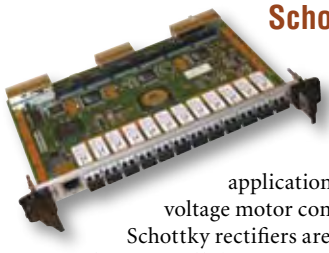


Schottky Rectifier Family Features QPL-Certification

The Qualified Parts List (QPL) is the U.S. Department of Defense's list of qualified semiconductor products produced by qualified suppliers in accordance with MIL-PRF-19500 screening requirements. QPL Suppliers are audited periodically, thus assuring that all customers receive products that meet government standards. International Rectifier has introduced a series of high-reliability Schottky rectifiers in accordance to the Defense Supply Center Columbus (DSCC) Qualified Products List (QPL). These QPL devices target high-reliability applications in switching power supplies (SMPS), satellite power distribution systems, resonant power converters and low-voltage motor control.

Schottky rectifiers are used primarily in the output stage of a switching power supply. Delivering very low forward voltage drops (Vf) and fast turn-off characteristics (trr), the devices minimize conduction and switching losses in power supply designs. The devices feature a +45V to +100V reverse-voltage range, a 0.69V to 1.3V forward-voltage range, and 10A to 35A current rating. Available in surface-mount and through-hole packages, the devices are screened to JANTX, JANTXV and JANS levels per MIL-PRF-19500/MIL-STD-750, offering customers the highest reliability available. The QPL Schottky rectifiers are available immediately. Pricing begins at $125 each for the JANTX1N6660CCT1 in 1,000 piece quantities.

International Rectifier, El Segundo, CA. (310) 726-8512. [www.irf.com].

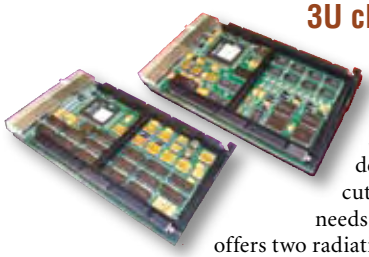
USB Modules Provide Multi-Function I/O Solution

While not an overnight success in embedded applications—much less in embedded military systems—Universal Serial Bus (USB) has begun to see acceptance in both those arenas. Along those lines, Advantech has introduced three modules: the USB-4750, a 32-channel isolated digital I/O USB module; the USB-4751, a 48-channel TTL digital I/O USB module; and the USB-4751L, a 24-channel TTL digital I/O USB module. These modules have been specifically designed for rugged environments and include USB connectors with screw fasteners and DIN-rail mounting kits. They draw power directly from the USB port and therefore do not require an external power supply. Relying on the plug-and-play features of USB, these modules are so easy to use that users need less than five minutes to set up before acquiring data.

The USB-4750 has isolation protection of 2,500 VDC, making it suited for applications where high-voltage protection is required. It has 16 isolated digital inputs and 16 isolated digital output channels, supports 5~40 VDC isolated input channels, and has a high sink current on the isolated output channels (100mA/channel). The USB-4751 (shown) has six 8-bit I/O ports, whereas the USB-4751L has three 8-bit ports.

Advantech, eAutomation Group, Cincinnati, OH. (513) 742-8895. [www.eAutomationPro.com].

3U cPCI I/O Cards are Ready for Space Duty



When something goes wrong in space, problems quickly spell disaster. That's why boards designed for such use need to be a cut above the rest. Serving such needs, Aitech Defense Systems now offers two radiation-tolerant 3U, CompactPCI (cPCI) I/O cards. The analog S930 and digital S940 FPGA-based cards both feature triple redundant buffer memory and can generate interrupts, eliminating the need for a more costly onboard processor to manage the I/O. The conduction-cooled cards come standard with component screening to NASA GSFC 311-INST-001A Level 2, making them suited for applications such as the International Space Station, where they are currently in use today.

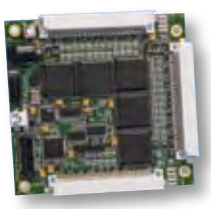
The S930 employs a 12-bit A/D converter that enhances subsystem sensitivity by detecting minute changes in externally sensed voltages. It also features 64 analog channels (51 inputs, two outputs and 11 bus voltage monitors) as well as a low pass filter with cutoff frequency below 50 Hz on all inputs. The S940 incorporates an H-bridge that efficiently provides pulse code modulation (PCM) control and drives the DC motors, and its four RS-422 inputs and 12 RS-422 outputs help DC motor controls sense how the motor is operating. Pricing for the S930 is $10,000, and for the S940 is $13,170 in OEM quantities.

Aitech Defense Systems, Chatsworth, CA. (888) 248-3248. [www.rugged.com].

StackableUSB SBC Boasts Extended Temp Range

Marrying the tried and true size and stacked concept of PC/104 with the fast, ubiquitous USB interconnect, the emerging StackableUSB specification seems to have hit a home run. Military developers are eyeing this technology as a migration path from ISA-based PC/104. Creator of StackableUSB, Micro/sys, has rolled out the newest addition to its StackableUSB line of SBCs. Called the SBC1496, the board operates from -40° to +85°C and provides I/O expansion via StackableUSB peripherals. In addition to PC-compatible features, such as SVGA and dual serial ports, the new model also includes four USB 2.0 high-speed (480 Mbit/s) ports, two USB 1.1 full-speed ports and 100BASE-T Ethernet support.

With up to 64 Mbytes of SDRAM, CompactFlash and full AT-compatibility, high-performance control systems can be implemented on this stackable embedded form-factor (PC/104-size) SBC. The SBC1496 is implemented with the STPC Atlas processor, which offers speeds up to 133 MHz, on-chip cache, 64-bit DRAM access and hardware floating point. When I/O expansion is needed, the StackableUSB interconnect architecture enables the control of up to five StackableUSB peripheral devices in a rugged, bolt-together platform. The basic SBC1496 starts at $385 in single quantity. The extended temp version is available starting at $435. Significant OEM discounts are available.



Micro/sys, Montrose, CA. (818) 244-4600. [www.embeddedsys.com].

Rugged 2D/3D Systems Target Vehicle-Based, Man-Wearable Visual Computing

Computers designed for real-time, tactical operation in ground vehicles, aircraft and naval vessels must meet Mil-Spec ruggedization levels, as well as rapid insertion and removal needs for security and mission-specific updates. Two new small form-factor 2D/3D tactical/deployed visual computers from Quantum3D have just those needs in mind, and a third is designed for man-wearable applications. Models 6300, 3500 and TL join Quantum3D's Thermite TVC-2.0 family. The 6300 was designed for ground vehicles, aircraft and naval vessels. A companion Vehicle Mounting Dock (VMD) features an integral, rugged blind-mate connector and a host of vehicle-specific I/O. The 6300 conforms to MIL-STD-810F and 461E, as well as 1275B and 704, enabling it to operate with 28 VDC for mil vehicles.

The Model 3500 is optimized for vehicle-based applications where fixed mounting options are permissible and mounting space, power and weight are constrained. Like the 6300, the 3500 has standard and optional I/O capabilities, solid-state drive options and support for 28 VDC vehicle power. The Model TL is among the smallest tactical visual computers available, weighs only 0.75 kg and is PC compatible. Pricing for the Thermite TVC-2.0 Model TL is $5,750.

Quantum3D, San Jose, CA. (408) 361-9999. [www.quantum3D.com].

Intel Core 2 Duo AMC Targets Mil Comms

Advanced Mezzanine Cards provide the modularity needed in many demanding military communications systems. A single-wide AMC from Mercury Computer Systems combines a dual-core Intel processor and an FPGA for flexible switch fabric connectivity. The Momentum Series AXA-110 is well suited to the role of processing and communications heart of ATCA or MicroTCA systems. The AXA-110 delivers up to 40 Gbits/s of I/O through the FAT pipes.

At a core speed of 1.5 GHz and with a thermal design power of 17 watts, the AXA-110's Intel Core 2 Duo processor L7400 provides leading energy-efficient performance for small form-factor embedded platforms and enables high-performance implementations of 64-bit architecture. Using a Xilinx Virtex-5 FPGA, the AXA-110 connects to up to 16 high-speed serial lines totaling 40 Gbits/s.

The AXA-110 supports registered DDR2-400 SDRAM with ECC. Up to sixteen lanes of switched fabric interfaces are implemented in multiple configuration options using Xilinx Virtex-5 FPGAs in the FAT pipes region on the AMC.1/AMC.2/AMC.4-compliant fabric interface. Two 1000Base-BX Ethernet ports and two SATA interfaces are provided in the common options region. Pricing starts at $4,495 for a single board. Discounts are available on higher volumes.

Mercury Computer Systems, Chelmsford, MA. (978) 256-1300. [www.mc.com].

3U CompactPCI Card Provides GPS, GSM

In a variety of wireless, mobile military communications, such as transmitting, tracking and acquiring data, exceptional communications ability is needed in situations where signal strength is very low but high reliability is a must. A 3U, single-slot CompactPCI interface card from MEN Micro is equipped with a highly sensitive, 12-channel parallel GPS receiver and a GSM device. The GPS and GSM devices are optically isolated from other functions for increased reliability. The F210 GPS/GSM/UART interface card supports GSM 850, EGSM 900, GSM 1800 and GSM 1900 frequency bands, as well as the NMEA 0183 protocol.

The F210 has an extended operating temperature range of -40° to +85°C and a conformal coating for use in harsh environments.

Two SA-AdapterT slots are included for serial interfaces with RS-232/422/485 line drivers, with or without optical isolation. The board can accommodate three additional SA-Adapters for user-defined functions. Reverse SMA connectors provide the physical interface to the external GPS and GSM antennae. Pricing for the F210 is $1,719.

Men Micro, Lago Vista, TX. (512) 267-8883. [www.menmicro.com].

Module Targets Embedded Control, Data-Logging Apps

Equipped with 10/100 Ethernet connectivity, GPIO with onboard analog input and serial flash memory, a new module family from Rabbit Semiconductor is powered by the Rabbit 4000 microprocessor running at up to 58.98 MHz. The RCM4200 RabbitCore features hardware DMA, quadrature decoder, up to 35 GPIO lines shared with up to five serial ports and four levels of alternate pin functions. It targets applications such as embedded data-logging, remote device monitoring and control and serial-to-Ethernet communications.

The RCM4200 comes in two flavors, the RCM4200 and the RCM4210, with varying processor speed, analog availability and serial flash size. The RCM4200 version has 8 Mbytes of onboard serial flash memory (4 Mbytes for the RCM4210), optional 8-channel analog input for simple interfacing to a wide variety of sensors and an operating temperature range of -40° to +85°C for applications in mobile or industrial environments. The RCM4200 Development Kit includes the higher-speed RCM4200, a development board and the latest Dynamic C integrated development software with samples and libraries. In quantities of 100, the RCM4200 is priced at $89 and the RCM4210 at $81. Pricing for the RCM4200 development kit is $269.

Rabbit Semiconductor, Davis, CA. (530) 757-8400. [www.rabbit.com].

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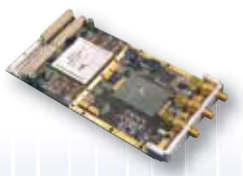

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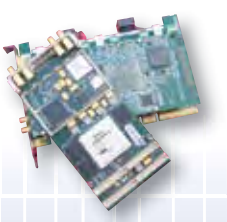

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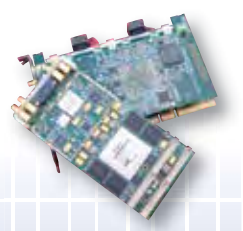

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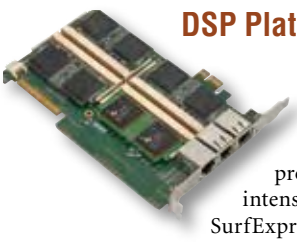
Core 2 Duo-Based Mini-ITX Board Has Dual Video Outputs

In response to demand in high-performance applications for a simplified system board combining robust computing power, a smaller footprint, lower power and increased product longevity, American Portwell Technologies has released the WADE-8056, an Intel Core 2 Duo-based Mini-ITX embedded system board (ESB). The 170 mm x 170 mm board's dual video outputs can drive two displays simultaneously at 2048 x 1536 maximum resolution (1920 x 1080 for HDTV). The board utilizes the Intel Q965 GMCH and 8280 1HB ICH8DO chipset to support Intel's 1.066 GHz Core 2 Duo and Pentium 4/Celeron D processors.

The Q965 chipset includes the fourth-generation Intel integrated graphics controller and a Graphics Media Accelerator 3000 that supports widescreen LCD displays and accelerated DirectX 9.0c. System memory is up to 4 Gbytes of 533/667/800 MHz dual-channel DDR2 SDRAM. Other features include a Gigabit Ethernet LAN port, PCI and mini-PCI expansion slots, four SATA ports with data transfers of up to 3 Gbits/s, four COM ports, GPIO, RAID (0,1,5,10) and six USB 2.0 ports. Linux and Windows are supported. Pricing is $330 per unit.

American Portwell Technologies, Fremont, CA. (510) 403-3399. [www.portwell.com].



DSP Platform Targets Mobile, Converged Telecom Apps

Developers of converged audio/video/data/VoIP equipment for military applications need a high-capacity, programmable platform for the processing-intense communications applications. The SurfExpress/PCIe—a DSP farm with VoIP, audio, video and data processing capabilities in a PCI Express form-factor—fills those needs. The single-lane, half-length, full-height board is optimized for mobile applications. With two Gigabit Ethernet ports and a computer telephony bus for additional TDM interfaces, the SurfExpress/PCIe meets the requirements of V2oIP enterprise-scale media servers, media gateways, 3G-324M video servers, Multimedia Messaging Service Center content adaptation engines and computer/telephone integration applications.

The board supports 1,088 voice ports and up to 224 low-resolution video ports on a single PCI slot. Each SurfDocker plug-in module, which supplies the PCIe carrier card with DSPs, carries up to four pairs of mixed types of DSPs, including Texas Instruments' TMS320C64x communications infrastructure optimized DSPs. Up to four SurfDocker modules can be plugged into a single SurfExpress/PCIe. The board comes with the company's SurfUP media processing software. Depending on configuration, pricing is $3/port for voice and $80/port for video.

Surf Communication Solutions, Arlington, MA. (866) 644-3379. [www.surf-com.com].

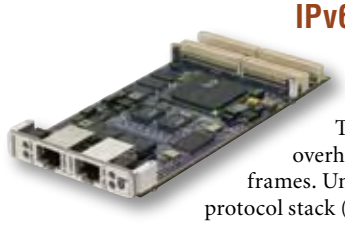
Ultra 320 SCSI Controller Supports Two Channels

The 4972 dual-channel SCSI Ultra 320 controller from Technobox supports two channels, one directed to the 68-pin SCSI front-panel connector, the other to the rear I/O PN4 connector. Termination, which is provided for each SCSI bus, automatically configures to support either single-ended or LVD devices. The board's default termination is active, but termination state may be changed by reprogramming the module.

Built around the LSI 53C1030, the 4972 features a 16 Kbit serial EEPROM, used to store user-configurable parameters by the LSI BIOS. A 512K x 8-bit flash memory holds the BIOS for Intel platforms and the BIOS is burned in the flash. A 32K x 8-bit non-volatile RAM holds mirroring data as required by the LSI logic firmware. LEDs on the body of the board convey activity status. Two indicate SCSI channel activity, another shows ARM processor heartbeat, and an additional two LEDs indicate that termination voltage is available at each SCSI interface. The 4972 lists for $695, and quantity discounts are available.

Technobox, Lumberton, NJ. (609) 267-8988. [www.technobox.com].

IPv6-Compliant TCP/IP Offload Engine Takes Aim at SIGINT

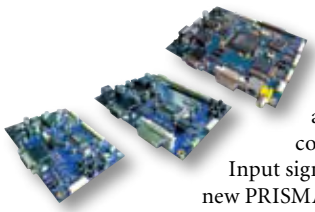


For high-performance, real-time systems, such as radar, sonar, SIGINT and data acquisition, the software-based approach to implementing network stack protocols, including IPv6, can quickly run out of gas. A TCP/IP offload engine (TOE) from Critical I/O offers complete hardware offload of IPv6 connections in a PMC form-factor.

The Critical I/O XGE4032 PMC offers 442 Mbytes/s sustained wire-speed throughput, ultra-low 1% host processor overhead, low 6 microsecond latency and deterministic behavior of +/- 1 microsecond variation typical, with no dropped frames. Unlike software stack implementations, the company's Silicon Stack Ethernet technology offloads the entire TCP/IP protocol stack (10/100/1000 Ethernet, TCP, UDP, IP, iSCSI and RDMA) in dedicated silicon.

An integrated firmware-based protocol engine permits easy protocol extensions and customization. The XGE4032 processor interface features a dual-channel design in conduction-cooled PMC versions. Options include copper or optical versions. Driver support for standard OS platforms as well as real-time VxWorks and RT Linux are available. A comprehensive library for applications that bypass the OS or have no OS runs on embedded processor families such as PowerPC, Intel/AMD x86 and DSPs. Low quantity pricing starts at $2,479.

Critical I/O, Irvine, CA. (949) 553-2200. [www.criticalio.com].



RGB/DVI/Video Converter Boards Boast Analog Control

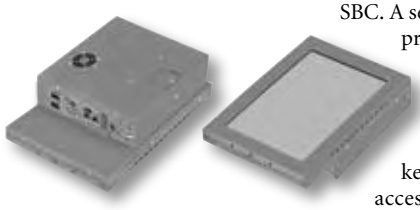
A new series of RGB/DVI/video converter boards provides a range of cost-effective solutions with analog control for connecting TFT LCDs to standard graphics and/or video interfaces. Input signals are automatically converted by Apollo Display Technologies' new PRISMA II boards into TTL or LVDS signals, scaled to the appropriate TFT resolution. They support TFT displays from 6.4-in. to 82-in. diagonal with 6-bit and 8- bit color depth, as well as single- and dual-channel LVDS. The PRISMA II board is optimized for multimedia applications, the PRISMAeco II connects TFT displays to RGB analog and DVI standard graphics interfaces, and the compact PRISMAeco Slim connects TFT displays from VGA to the RGB analog standard graphics interface.

The PRISMA II board provides state-of-the-art features including Component Video-In, support of resolutions up to full HD, WUXGA (1920x1200), improved video quality and de-interlacing, improved auto-adjust, power supply options up to 24V, and an advanced human/machine interface option. PRISMAeco II and PRISMAeco Slim support TFT displays from VGA to SXGA resolution, with TTL and LVDS output. Pricing starts at $51 for the PRISMAeco II in production quantities.

Apollo Display Technologies, Ronkonkoma, NY. (631) 580-4360. [www.apollodisplays.com].

Rugged Panel Computer Sports NEC Flat Panel Display Module

For rapid deployment of human-machine interface and operator control applications, rugged panel computers can provide an application-ready solution. Ampro Computers' new ReadyPanel 10 all-in-one panel PC is equipped with the NEC LCD Technologies NL10276BC20-04 10.4-in. XGA color TFT flat panel display module, which provides 1024 x 768 resolution and includes an integrated touch screen. The ReadyPanel 10 includes a standard EPIC form-factor Pentium processor-compatible SBC. A selection of Ampro ReadyBoard SBCs are available with processor speeds ranging from 500 MHz to 1.4 GHz. Up to 1 Gbyte of DRAM can be configured.



Standard connectors are provided for easy access to USB ports, RJ-45 Ethernet ports, serial ports (DB9), CRT video ports (when required), PS/2 keyboard and mouse ports and audio ports. External access to the CompactFlash slot is through an EMI-protected cover. Options include a 2.5-in. HDD and CANbus. ReadyPanel 10 supports embedded Linux and Windows XP Embedded, XP Pro or CE 5.0. It comes with embedded Linux on 256 Mbytes of CompactFlash storage and 256 Mbytes of system memory. Pricing starts at $1,599 in volume quantities.

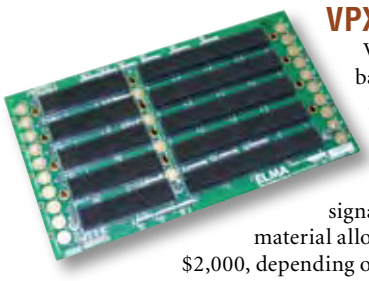
Ampro Computers, San Jose, CA. (408) 360-4324. [www.ampro.com].

Ultra-Low Phase Noise RF Oscillator Aims at Radar

Newer-generation radar systems capable of detecting stealthy targets need small, lower phase noise and very stable high-performance frequency sources. In particular, the development of ultra-stable frequency sources at 500 MHz, a reference for L band and X band sources, is highly desirable. An ultra-low phase noise RF oscillator from Temex, the SR W150, delivers 300 MHz to 600 MHz frequency, has a phase noise floor of -175 dBc/Hz and is provided in a package measuring only 2 in. x 2 in. x 0.8 in.

The oscillator's frequency is stabilized by temperature control and external control voltage. Stability is 1 ppm in the 0° - 50°C temperature range with a target of -30° to + 70°C. Aging is only 1 ppm/year. Once the oscillator has been adjusted in the factory, it does not require additional calibration. Pricing depends on quantity. Basic price for a single unit is $4,000.

Temex, Sophia-Antipolis, France.
+33 4 97 233 000. [www.temex.com].

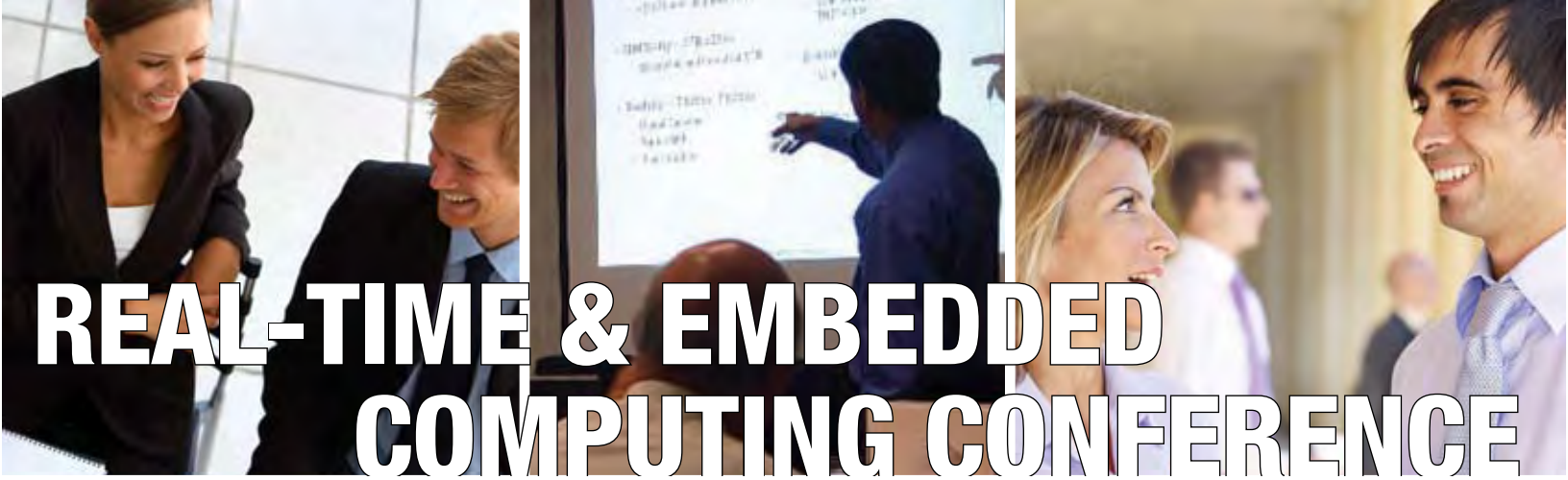


VPX Backplane Has Five Slots

VPX (VITA 46) delivers improved speed, power and flexibility for military embedded systems, yet maintains backward compatibility with legacy VME technology via preservation of the VMEbus 6U mechanical form-factor and through-mapping of the current VMEbus signals to the VITA 46 connectors. As a result, demand for this technology is growing rapidly. With that in mind, Elma Electronic has released a five-slot VPX backplane.

The backplane was designed with a 20-layer controlled-impedance stripline design and features a mesh topology with a theoretical slot-to-slot bandwidth of over 5,000 Mbytes/s. To ensure optimal performance, signal integrity analysis was performed on the backplane. Fabrication with the higher-grade commercial FR408 material allows excellent performance, even at high signal frequencies. Pricing for the five-slot VPX backplane is under $2,000, depending on volume and configuration requirements.

Elma Electronic, Fremont, CA. (510) 656-3400. [www.elma.com].



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Coming Next Month

COTS JOURNAL

- *Multicore Processors for the Military.* The road maps of the leading processors show that all roads lead to architectures sporting multiple CPU cores on the same device. Some military applications have an immediate need for the level of computing muscle such devices provide. Compute-intensive applications such as sonar, radar, SIGINT and UAV control systems fall into that category, along with several others. But because the trend is fundamental across all processor vendors, issues surrounding multicore processing must be faced by all high-end computing applications in the near future. This feature section delves into the board-level solutions available in multicore processing and how they're transforming military systems.
- *DRAM and Flash Tech Trends.*Changing even faster than microprocessors, memory ICs like DRAM and flash evolve at rates that are hard for anyone to keep up with—let alone the extremely long design cycles inherent to the military realm. This section updates readers on the latest technology and product developments in both flash memory and DRAM, and analyzes how these will affect tomorrow's military system designs.
- *1553 Boards.*The 1553 interconnect is found in almost all existing military aircraft and is still being designed into new aircraft as well as tanks, howitzers and missiles. At 1 Mbit/s half duplex, 1553 is relatively slow, but it is reliable in the presence of noise and distortion. This Tech Focus section updates readers on the latest trends in 1553 board-level products, and includes a focused product album of representative 1553 boards in various form-factors such as PC/104, cPCI, PMC, PCI and more.
- *SPECIAL SUPPLEMENT: Payloads for UAVs.* This special supplement will examine the issues and challenges that engineers and program managers are facing in finding the best enclosure, embedded board architectures and fabric solutions that match up with the needs of various UAV payload requirements. Readers gain insight into the problems, challenges and form-factor changes that are driving today's UAV payload system designs. Payloads options for UAVs—both large, small and in between, will be looked at including GlobalHawk, Predator, Shadow, Raven, Hunter, Hurricane, FireScout, BAMs and others.

Editorial

Jeff Child, Editor-in-Chief

Meeting with embedded board vendors and real-time software firms at the Embedded Systems Conference (ESC) Silicon Valley tradeshow earlier this month got me thinking about an inherent tension that's ever-present in the embedded technology realm. I'm referring to the struggle between the desire to "start from scratch" with new technology, or to evolve or leverage existing technology to solve military system design requirements. The military—with its aversion to risk and inherent long design/development cycles—usually tends to lean heavily toward the existing technology side. That said, every category of technology comes up to transition phases eventually, and change eventually comes, albeit slowly.

Scratching the "Start from Scratch" Itch

My first example along those lines is the new StackableUSB specification introduced by Micro/sys last month. It defines a standard for stacking I/O boards onto a single board computer using the popular USB 2.0 interface. At ESC, Micro/sys showcased the StackableUSB effort—even investing in a separate booth for StackableUSB—and promoting it as independent of the PC/104 Embedded Consortium. Indeed, the rugged Samtec connector used in StackableUSB overlaps the same spot that the ISA-based connector occupies in PC/104. So it clearly signifies a break with the past.

Perhaps "start from scratch" is poor characterization in this example. Certainly USB is a very well established bus. That said, USB's application as a stackable board-to-board interconnect is brand new—or from scratch, to carry my metaphor forward. At the show I talked with Micro/sys President Susan Wooley about some of the motivations behind StackableUSB. Speed, she said, was a major one. USB high bandwidth makes it much more suited than ISA bus for supporting today's high-speed A/D and DAC data rates. Also important, Wooley explained, is the trend toward ISA's exclusion from new chipsets. This impending extinction of ISA, says Wooley, is sure to have a negative impact on the currently healthy, but aging ISA-oriented PC/104 market.

Most of the PC/104 board vendors I talked to at ESC had positive reactions to the StackableUSB initiative. But not all shared the view that ISA is nearing extinction. For its part, Ampro Computers, while offering several non-PC/104 product lines, sees no rapid demise ahead for its PC/104 product offerings. Joanne Mumola Williams, CEO of Ampro Computers, pointed out that ISA remains a critical component for implementing real-world control I/O found in many military applications. And PC/104, she said, is one of the few architectures that continues to offer support for ISA bus.

In a totally different area of the ESC vendor spectrum, I found yet another example of that same tension between "start from scratch" and "leveraging what's proven to work." This one is in the arena of secure embedded software—a topic of keen interest to military programs such as Future Combat Systems, for which LynuxWorks was selected as the OS vendor. Real-time OS vendor LynuxWorks, at a technology symposium it put on at ESC, revealed plans to develop a new RTOS for security-critical systems.

Called LynxSecure, the product supports the multiple independent levels of security (MILS) architecture, which entails a "separation kernel" with partitions that ensure data isolation, information flow control and damage limitation. It will include a virtual-machine monitor capable of running multiple operating systems. Interestingly, LynuxWorks plans to design it "from scratch"—or "from the ground up" to use their terminology—to conform to the highest possible assurance level: Common Criteria Evaluation Assurance Level (EAL) 7. Gurjot Singh, CEO of LynuxWorks, told me that the "from the ground up" strategy was essential to any serious aim at conforming to EAL 7.

What I found intriguing is that the LynuxWorks announcement seems to carry an implied knock on its rival Green Hills Software's direction for high-assurance certification. Green Hills Software's Integrity RTOS was designed with and has employed the separation kernel concept for over a decade. Integrity is a MILS-based RTOS and was first deployed on the B-1 stealth bomber. In contrast to LynuxWorks, Green Hills took an existing product, Integrity-178B, and submitted it as the first RTOS to undergo testing by the National Security Agency for the ISO/IEC Common Criteria Evaluation Assurance Level (EAL) 6. Like EAL 7, EAL 6 requires validation by formal methods. Meanwhile, Wind River Systems offers a version of its VxWorks RTOS that's compatible with the ARINC 653 specification standard for time and system partitioning, as well as DO-178B. (For more details on MILS see the Wind River article on page 54 in this issue.)

So which is the better approach? Start from scratch or evolve and rely on what exists? Well, I'm afraid I have no wisdom to offer on that question. That judgment call is particular to the application and the market motivations of the vendor. But there are a lot of cases cropping up these days where functionality designed in at the ground floor is providing some clear advantages. I would put the Line Replacement Module (LRM) aspects of the emerging VITA form-factor VITA 46 (VPX) in that category.

Also referred to as two-level maintenance, the idea of LRMs—board-level subsystems that can be hot swapped out of a system platform (aboard a tank, ship or aircraft), rather than replacing a whole box-level system—has become a high priority. Board vendors and primes can and do offer that capability today using very expensive approaches with highly customized connectors to modify ordinary VME boards. With VPX and VPX REDI, support for LRM use was designed in from the beginning and is therefore much more cost-effective than adding after-the-fact features like protection against electrostatic discharge and provisions for a consistent failure indicator. Score a victory there for the "start from scratch" itch scratchers. ▮▮

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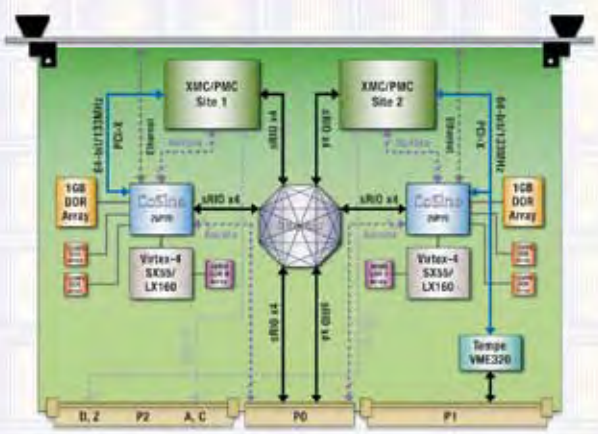

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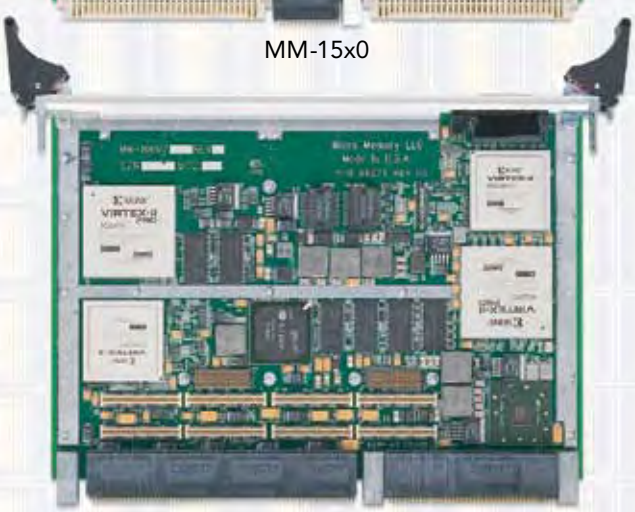

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